# COMP3211/9211 2003 Assignment 3

# Multi-cycle Processor

**Contribution to final assessment: 13 $^{1}/_{3}$ % (as revised for Assignments 1 & 2 as well)**

**Due: 4.30 PM, Friday, 7 November**

## Overview

The goal of this assignment is to transform an existing single cycle processor design into a five-stage multi-cycle design and to simulate and compare the operation of the enhanced design with that of the original design when executing a given program.

## Detailed Requirements

You are given the design, documentation, and simulation results for a single cycle processor (these are available from the COMP3211 web site as links to A3 source and A3 document respectively). This design and documentation were submitted as the solution for an assignment for COMP3211 in 2002 and judged to be of good quality. The original problem that was to be solved with the single cycle processor design is described on Page 1 of the document. It is your job is to modify the design and program, and to submit an enhanced design and report.

**Notes on provided materials:** The source and documentation provided to you is lengthy. It would be appreciated if you do not print these in total, but rather only print extracts as necessary. The provided source and documentation are provided on an as is basis. Specifically, they are not guaranteed to be correct. It is your responsibility to correct any deficiencies you notice that may cause problems in carrying out the requirements for this assignment. You may use any modules given to you as source as long as you attribute authorship appropriately and outline the modifications you made to such modules. *It should also be noted* that queries relating to the materials provided should be directed to the **`comp3211_tutor-list`**, not to the original authors. Reasonable queries will be answered from there.

You are required to make changes and complete a redesign as follows:

1. Enhance the program to save the calculated result at location `N+1`. The instruction set thus needs to be augmented with a **`sw`** instruction. Include a copy of the amended program in your report.

2. You are required to draw a block diagram of the datapath after it has been transformed into a five-stage multi-cycle design. Indicate the locations where you would insert registers. Clearly label **all** control and status signals required by the final design.

   **Note:** You are only required to provide one block diagram with your report, so it may be sensible to incorporate subsequent requirements into this diagram.

3. Construct a micro-programmed controller for the revised datapath:
    a. Describe the register transfers needed to complete each micro-operation for each instruction type.
    b. Construct the micro-program needed to implement the augmented instruction set.
    c. Draw a block diagram of the micro-program controller indicating which status signals and inputs it uses and which control signals it provides.
    d. Construct a VHDL model of your controller.

4. Transform the provided `processor` model into the multi-cycle design you have described:
    a. Delete the delays in the leaf components of the provided VHDL models – these include those in the `mux, alu, pc, instructionmem, datamem,` and `regfile.` Your multi-cycle design should assume a delay of 7 ns per stage.
    b. Insert stage registers where necessary.
    c. Include the new controller.

5. Produce a simulation waveform that clearly illustrates and demonstrates the correct operation of the enhanced datapath on the original program after it has been modified to store the final result. This means you will need to display all relevant internal signals that change from cycle to cycle.

6. Compare the performance of the enhanced datapath with that of the original datapath executing at 20MHz.

## Deliverables

You are required to produce a printed report that includes the above requirements. (The document provided as part of the specifications for this assignment serves as a good model of a high standard assignment report.)

A printed copy of the above deliverables including a title page identifying

(i) the assignment title: COMP3211/9211 2003 Assignment 3,
(ii) your Tutorial day & time,
(iii) your Tutor's name, and
(iv) the names and student numbers of the members of your group (for this assignment, you are expected to pair with another person from your tutorial group)

should be submitted to and marked RECEIVED by the student office by 4.30 PM, Friday, 7 November, 2003.

You are also required to turnin an ASCII file containing the text of your report and including your VHDL source code using the command **`give cs3211 a3-proc assign3.txt`** by 5.30 PM, Friday, 7 November, 2003.

Please refer to the course outline for an explanation of the penalties that apply for late or copied work.