Comp3211 Solution Week12

Usama Malik

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1 Question 1

1. Clock cycle time: This will be the critical delay, or, the longest path through the entire circuit. Be referring to the table on page 374 of the P&H book, the load instruction takes the longest time. This time is the sum of : instruction memory, pc, decode, register read, ALU, data memory and register write. From the data given, this is: 2 + 2 + 1+ 2+ 2+ 2+ 2 = 13ns. Hence the clock cycle time is: 13ns.
2. The 5 stages can be:

1. Instruction fetch. Read memory and add 4 to PC. Instruction memory read + adder = 4ns. Assuming the two operations are performed in a sequence.

2. Instruction decode and register fetch. 1 + 2 = 3ns. Assume that both registers can be simultaneously accessed.

3. execution, memory address computation, or branch completion. ALU. 2ns. For Jump type instructions, we just update the PC with IR[25-0] (Instruction Register). We assume that the ALU takes longer time than this.

4. memory access or R-type instruction completion. 3ns.

5. Memory read completion. 2ns.

The longest operation takes 4ns. Hence, the clock cycle time is 4ns.
3. For a single cycle machine, the CPI is 1.

For a multi-cycle machine: From Figure 5.42 of the text book, the number of cycles for each instruction is as follows: Load: 5, Store: 4, R-type: 4, Branch: 3, Jump: 3. Hence CPI is given by:

$0.2 \times 5 + 0.1 \times 4 + 0.65 \times 4 + 0.05 \times 3 = 4.15$.

2 Question 2

Removing the two registers A and B, the stages become:

1. Instruction fetch. Read memory and add 4 to PC. Total time = 2ns. Instruction memory read + adder = 4ns.

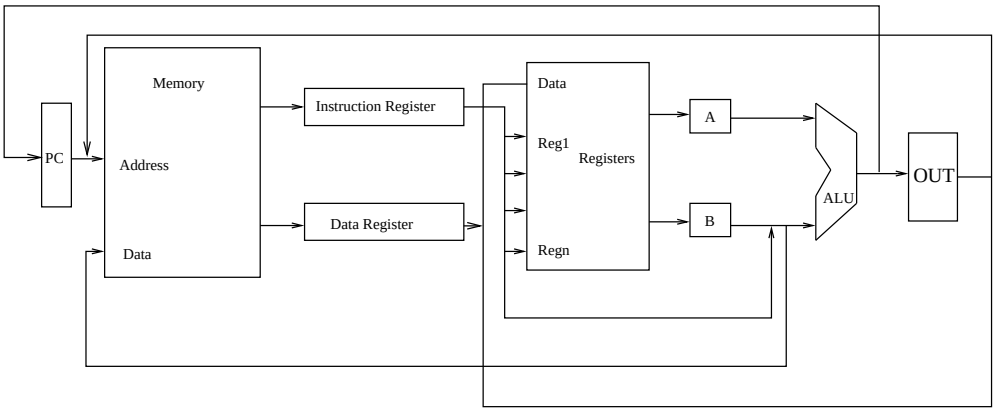

Figure 1: A high-level view of a multi-cycle machine (adopted from p378 of P&H)

2. Instruction decode execute: 1(Decode) + 1(ALU) . 1 + 4 = 5ns.
3. memory access or R-type instruction completion. 3ns.
4. Memory read completion. 2ns.

Hence the clock cycle time is now 5ns.
CPI:
load: 4, store: 3, jump:2, R-type:3 and CPI = $0.2 \times 4 + 0.1 \times 3 + 0.05 \times 3 + 0.65 \times 3 = 3.2$

3 Question 3

We cannot delete the instruction register as it might be needed at a later stage (such as for immediate type instructions). If we delete it, the data will be overwritten by the next instruction in the next cycle.

4 Question 4

Assembly Level Program:
add1 c, a, $0
addi a, b, $0
addi b, c, $0

Microprogram for *each* addi is :

Label	ALU Control	SRC1	SRC2	Reg Control	Memory	PC Write	Seq
Fetch	Add	PC	4		Read PC	ALU	Seq
	Add	PC	Extshft	Read			Dispatch
RFormat	Func Code	A	B				Seq
				Write ALU			Fetch

The program needs $4 \times 3 = 12$ cycles.

We can propose another solution as follows:
We assume that the two words, *a* and *b*, are in memory, and are adjacent, and the address of the first one is given by an immediate type instruction.

Label	ALU Control	SRC1	SRC2	Reg Control	Memory	PC Write	Seq
swap					Read ALU		Seq
				Write MDR			Seq
	Add	A	4				Seq
				ReadALU			Seq
			B	WriteALU			Seq
			Write MDR				Seq
	Sub	A	4				Seq
			Write MDR				Fetch

Note the use of the temporary register B to store one of the variables. This program needs 7 cycles.