COMP3211/9211 Computer Architecture
2004 S2 Laboratory Exercise 2 (VHDL2)
ALU Design & Simulation (Draft 15/08)

1 Goal

The goal of this exercise is to introduce trade-offs in building models at different levels of abstraction and trading accuracy for simulation speed. In doing so, you'll also develop VHDL and simulation skills while building a simple ALU model.

This exercise is due to Yalamanchili.

2 Exercise

Step 1

Start with the model of a single-bit ALU provided for you under the VHDL models link of the course web page. This model is constructed with concurrent signal assignment statements. Substitute this model with one that replaces all the concurrent signal assignment statements in the architecture body with sequential assignment (`if-then-else`) statements and a single process. The process should be sensitive to events on input signals `a`, `b`, `c_in`, and `opcode`. The process should use variables to compute the value of the ALU output. The last statement in the process should be a signal assignment statement assigning the ALU output value to the signal result. Use a delay of 10 ns through the ALU for both `result` and `c_out`.

Step 2

Analyze, simulate, and test this model, and ensure that all three operations (AND, OR, and ADD) operate correctly.

Step 3

Construct a VHDL structural model of a 4-bit ALU. Use the single-bit ALU as a building block. Use a ripple-carry implementation to propagate the carry between single-bit ALUs. Simulate and explain the output waveforms you obtain.

Step 4

Construct an 8-bit ALU using the 4-bit ALU as a building block. Use a ripple-carry implementation to propagate the carry between single-bit ALUs.

Step 5

Based on your construction, what is the propagation delay through the 8-bit adder? Generate a test case for each ALU instruction. Run the simulation for a period equal to at least the delay through the 8-bit adder.

Step 6

Rewrite the 8-bit model as a behavioural model without hierarchy. Use a single process and the following hints:

a) Inputs, outputs, and internal variables are all 8-bit vectors of type std_logic_vector.

b) Make use of variables to compute intermediate results.

c) Use the case statement to decode the opcode.

d) Do not forget to set the value of the output carry signal.

e) The propagation delay should be set to the delay through the hierarchical structural model.

Step 7

Test the new model.

Step 8

Qualitatively compare the two models with respect to the difference in the number of events that occur in the flattened hierarchical model and the single-level model in response to a new set of inputs.

3 Hand-in Exercise

At the start of your 3rd Lab Session in Week 06/07, please submit the following for marking:

a) A printout of your code from Steps 4 and 6;
b) A printout of your simulation waveforms from Steps 5 and 7; and
c) A typewritten response to the question posed in Step 8.