1. (a) Shown below is most of a listing file for a SRC program.. The program counter contains the number 1000 Hexadecimal. The source code for two instructions is not shown. On the lines headed .by "Part a" give the assembler code for the omitted instructions. A table of SRC op-codes is shown at the end of the exam. (12 pts)

   (b) Trace the execution of the program. On each line headed by "Part b" show the contents in hexadecimal of ***all*** registers and memory locations changed by fetching and executing the instruction. If an instruction is not fetched and executed, write "NFE" on the line. (18 pts)

40107005 = 0100 0000 0001 0000 0111 0000 0000 0101 = 8 0 8 7..5. The op-code is that of a branch instruction, 5 in the least 3 significant bits means this is a branch on minus. The Ra field is 0, the Rb field specifies register 8 and the Rc field register 7. The instruction is brmi r8, r7

The second instruction is 2240000c = 0010 0010 0100 0000 0000 0000 0000 1100 = 4 9..C the op-code is for a STR instruction using register 9. The address is the PC + 12 = 1020, which has the label X. The instruction is therefore str r9, X

			Part a	Part b
HexLoc	MachWord	Label	Source Code	
00000000	00000000		.org 1000H	
00001000	09c01020		ld r7, X	r7 ← 00000004h; PC ← 1004h
00001004	2a001014		la r8, next	r8 ← 1014h; PC ← 1008h
00001008	40107005		brmi r8, r7	Number in R7 is positive so PC ← 100c
0000100c	7a407000		neg r9, r7	R9 ← 4 = fffffffch PC ← 1010h
00001010	2240000c		str r9, X..	M[1020h] ← fffffffch, PC ← 1014h
00001014	f8000000	next:	stop	PC ← 1018h, RUN ← 0
00001018	00000000		.org 1020H	
00001020	00000004	X:	.dc 4	

2, Figure 1 shows part of the datapath for a single bus computer. (25 pts)
   (a) On the diagram, complete the datapath for the Z register.
   (b) On the diagram, draw all of the control signals that are needed for the Y and Z registers..
   (c) Why is the Y register needed?
   (d) Why is the Z register needed?
   (e) Show the Concrete RTN and the sequence of control signals needed to execute the SRC add instruction: add R0, R0, R1 **on this architecture**.

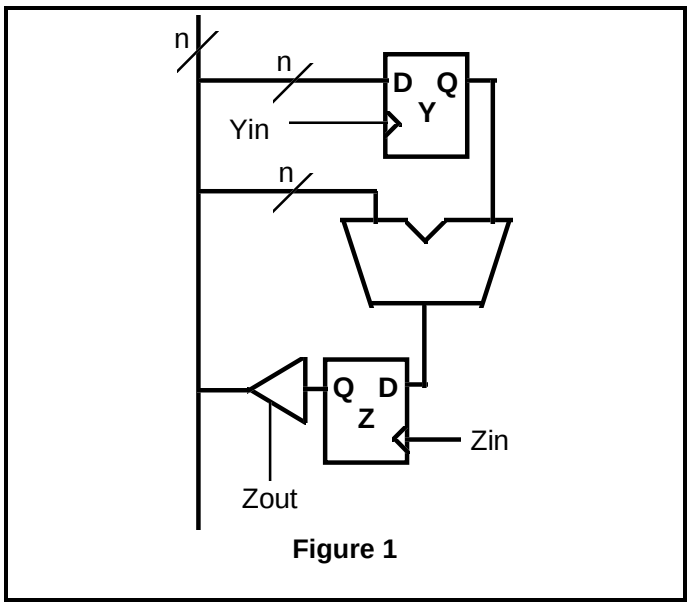


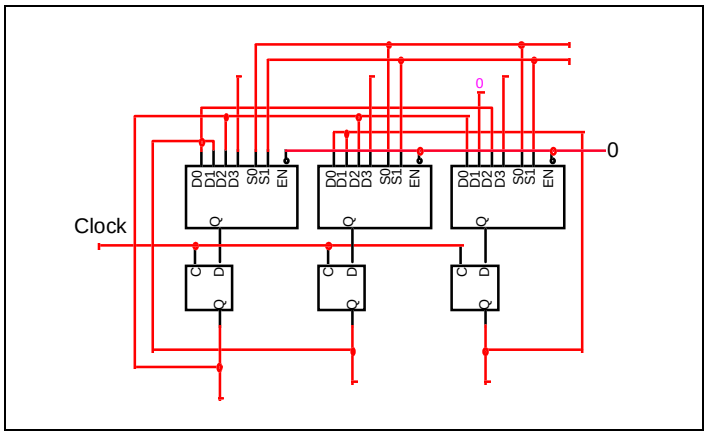
Figure 1

2. c The adder is a purely combinational circuit. It requires that both operands be presented at the same time, but only one operand can be on the bus at a time. The Y register is loaded with one operand and then the other is placed on the bus so that the adder can have both simultaneously.

d The Z register is used to capture the result since the bus is in use to supply one of the operands to the adder.

e Y ← R0 -- R0out, Yin; Z ← R1 + Y -- R1out, Zin; R0 ← Z -- Zout, R0in

3. Use multiplexers and Flip-flops to draw a 3 bit shift register that will perform a left circular shift when the select lines are 00, a left logical shift when the select lines are 01, a right arithmetic shift when the select lines are 10, and can be loaded in parallel when the select lines are 11. You need not show the gates that make up either the multiplexers or flip-flops, but you must label the multiplexers to show which input line is selected for each value of the select lines and you must indicate the type of flip-flop that you are using. (25 pts)



4. Figure 2 shows a circuit and its inputs. On the diagram draw the output waveforms for C and D. Show the number of gate delays in the outputs relative to the signal that caused the change in the output. (20 pts)

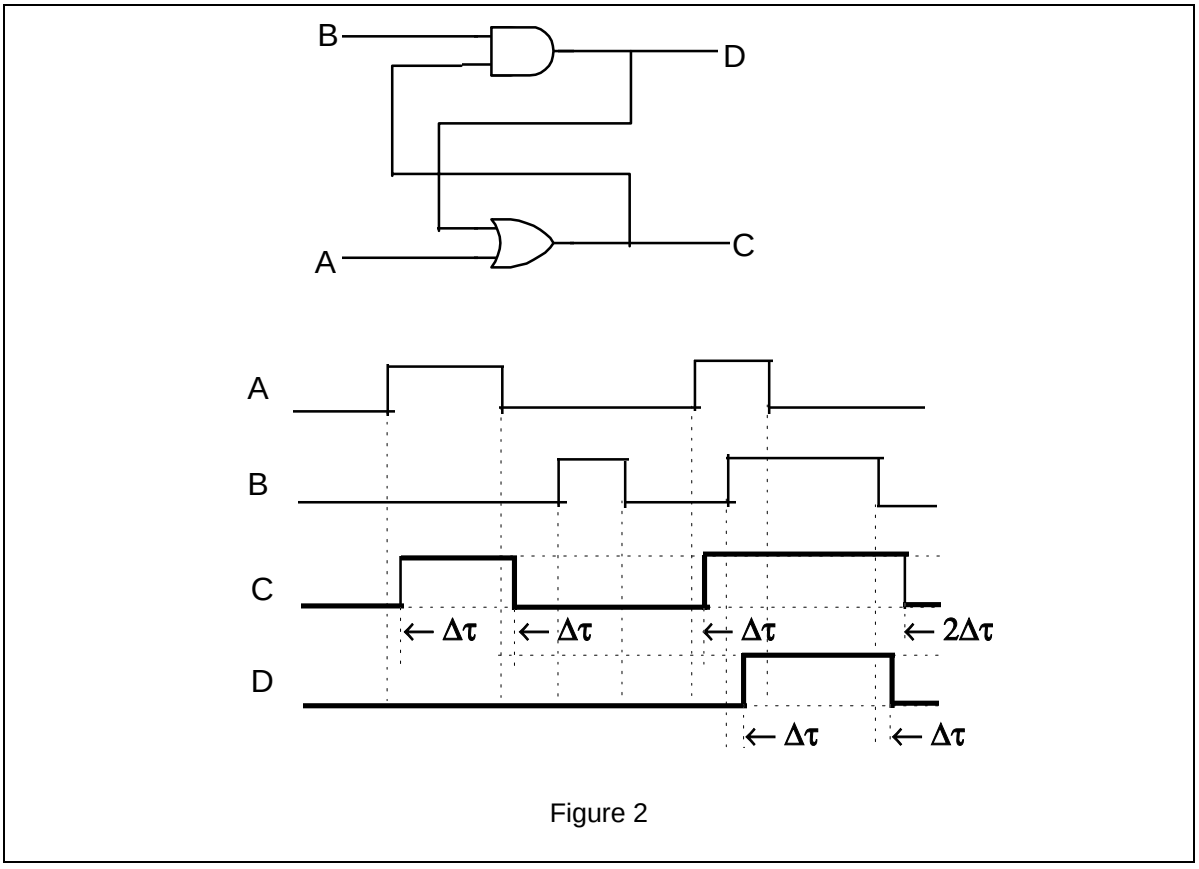


Figure 2