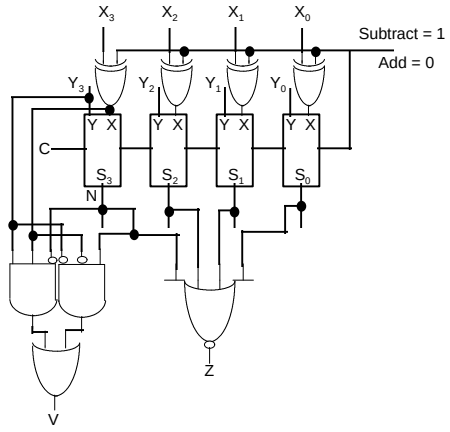
CS240 Midterm April 11, 2002 Answers

1. a Using full adders and any necessary gates, draw a circuit that will either add two 4 bit numbers X ($x_3x_2x_1x_0$) and Y ($y_2y_2y_1y_0$), or will subtract X from Y as controlled by a control line that is 1 for subtraction and 0 for addition. (15 pts.)
   b Show how to use the circuit above to generate the condition codes N, V, C, and Z (which you must define). (15 pts.)



2. Shown below is a SRC assembly language program that is executed.

		Location	
	.org 1000H		
endtest:	.dc -12345		
	.org 5000H		
	ldr r10, endtest	5000H	PC ← 5004H, r10 ← -12345
	lar r30, start	5004H	PC ← 5008H, r30 ← 500CH
	lar r20, end	5008H	PC ← 500CH, r20 ← 5018H
start:	brlmi r5, r20, r10	500CH	PC ← 5018H, r5 ← 5010H
	neg r10, r10	5010H	NFE
	br r30	5014H	NFE
end:	stop	5018H	PC ← 501CH, (Run ← 0)

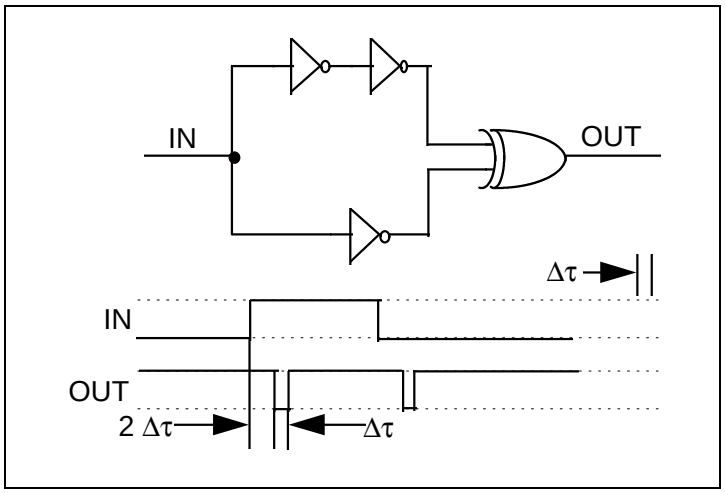
   a ***On the line next to each instruction that is actually executed***, show the contents of all registers that are changed as a result of ***fetching and executing*** the instruction. ***If the instruction is not fetched and executed, write "NFE".*** (15 pts.)
   b Show the Hex. values that are generated by the assembler for the lines of source code that are underlined above. See the table of "Op-Codes at the end of the exam. (15 pts.)

First convert 12345 to Hex. by dividing by 16 = 3039 H. Then form the 2's Complement 0011 0000 0011 1001 → 1100 1111 1100 0111 (2's Complement) → FFFFCFC7H (sign extended to 32 bits)

The op-code for the ldr is 2 and the register is r10 giving 00010 01010 The remaining 22 bits contain the displacement from the current value of the PC, 5004H, to "endtest" = 1000H. The difference is -4004H. To get the negative value form the 2's C and extend to 22 bits. 0100 0000 0000 0100 → 1011 1111 1111 1100. The complete instruction is therefore: 00010 01010 11 1111 1011 1111 1111 1100 = 12BFBFFCH.

The opcode for the brl is 9 and the 3 register fields contain 5, 20, and 10 giving 01001 00101 10100 01010. The low order 3 bits of the instruction are 101 indicating a branch when register 10 contains a negative number. This gives 01001 00101 10100 01010 0000 0000 0101 = 4968A005H.

3. Shown below is a circuit and its input waveform. On the diagram, draw the output. A gate delay is shown on the diagram. Label the output to indicate the number of gate delays from the change in the input that caused the change in the output. (15 pts.)



4. Shown below is the truth table for a function of four variables, b_3, b_2, b_1, and b_0. The truth table has been split in half to save space, but it represents a single table

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Hex	b_3	b_2	b_1	b_0	F		Hex	b_3	b_2	b_1	b_0	F	
0	0	0	0	0	1		8	1	0	0	0	0	
1	0	0	0	1	1		9	1	0	0	1	1	
2	0	0	1	0	0		A	1	0	1	0	d	
3	0	0	1	1	0		B	1	0	1	1	d	
4	0	1	0	0	1		C	1	1	0	0	1	
5	0	1	0	1	d		D	1	1	0	1	1	
6	0	1	1	0	0		E	1	1	1	0	0	
7	0	1	1	1	1		F	1	1	1	1	1	

a Use a Karnaugh map to derive the minimal sum of products. (15 pts.)

b Implement the function using only NAND gates (any number of inputs). In answering this question, you may assume that the inverted forms of the input variables are available and you need not show inverters. (10 pts.)