

Com2113 Syllabus

Spring 2002

Why study computer organization?

Digital Logic

- Combinational Logic
- Truth Tables
- Logic Gates
- Properties of Boolean Algebra
- Binary, Octal, and Hexadecimal Numbers
- Sum of Products and Logic Diagrams
- Product of Sums
- Positive versus Negative Logic
- The Data Sheet

- Digital Components
- Reduction of Two-Level Expressions
- Speeds and Performance
- Sequential Logic
- Registers
 - Register File
 - Shift Registers
- J-K and T Flip-Flops
- Counters
 - Ideal Ripple Up-Counter
 - Real Ripple Up-Counter
 - Ripple Down-Counter
 - Ripple Up-Down Counters
 - Synchronous Counters
- Design of Finite State Machines

Appendix A*

A.1

A.2

A.3

A.4

6.1

A.5

A.6

A.7

A.8 and On

Semiconductor

Manual

A.9

A.10

A.11

A.12

A.16

Notes

Notes

A.13

A.17

Notes

Notes

Notes

Notes

Notes

A.14

The General Purpose Machine

- The general Purpose Machine
- The User's View
- The Machine/Assembly Language Programmer's View
- The Computer Architect's View
- The Logic Designer's View
- Historical Perspective
- Trends and Research

Chapter 1

1.1

1.2

1.3

1.4

1.5

1.6

1.7

Machines, Machine Languages, and Digital Logic

- Classification of Computers and Their Instructions
- Computer Instruction Sets
- Informal Description of the Simple Risc Computer, SRC
- Formal Description of the SRC using Register Transfer Notation, RTN
- Describing Addressing Modes with RTN
- Positive and Negative Numbers
- Register Transfers and Logic Circuits from Behavior to Hardware

Chapter 2

2.1

2.2

2.3

2.4

2.5

6.1.2

2.6

Assembly and Assemblers

- What is an Assembler
- Assembly Language Structure
- Tasks of the Assembler

Appendix C

C.1

C.2

C.3

* All section designations refer to "Computer Systems Design and Architecture", by Heuring and Jordan, Prentice Hall, 1997 unless otherwise stated.

Some Real Machines

Machine Characteristics and Performance
RISC versus CISC
A CISC Microprocessor: The Motorola MC68000
A RISC Architecture: The SPARC

Chapter 3

3.1
3.2
3.3
3.4

Processor Design

The Design Process
A 1-Bus Microarchitecture for the SRC
Data Path Implementation
Logic Design for the 1-Bus SRC
The Control Unit
The 2- and 3-Bus Processor Designs

Chapter 4

4.1
4.2
4.3
4.4
4.5
4.6

Processor Design -- Advanced Topics

Introduction to Pipelining
Instruction Level Parallelism
Microprogramming

Chapter 5

5.1 & 5.1.1 only
5.2
5.3

Computer Arithmetic and the Arithmetic Unit

Fixed Point Arithmetic
Seminumeric Aspects of ALU Design
Floating Point Arithmetic

Chapter 6

6.2
6.3
6.4

Memory System Design

Introduction: The Components of the Memory System
RAM Structure: The Logic Designer's Perspective
Two-Level Memory Hierarchy
The Cache

Chapter 7**

7.1
7.2
7.4
7.5

** Depending on Time Constraints