The speakers are expert practicing professionals in the respective areas. More details of the tutorial and biographies of the speakers are available from the VDAT website - http://vlsi-india.org/events/vdat2009/index.html

Information
Please watch updates on VDAT at http://vlsi-india.org/ The idea behind the VLSI Design And Test (VDAT) Symposium is to promote Research and Development on all aspects of VLSI in India. This symposium is a forum for free discussion of hot and emerging topics in VLSI. It provides a meeting place for VLSI professionals working in India and abroad. We have been holding this event since 1998, and the participation in the event has steadily gone up every year. The VLSI Industry in India and academic community working in the area of VLSI has provided immense support to the symposium.

VDAT is sponsored by the VLSI Society of India. Please consult http://vlsi-india.org/vsi/ for more information on goals, activities of the VLSI Society of India, you can download the form from http://vlsi-india.org/vsi/membership/index.shtml (form is included at the end of this document).

For a larger image of the route map: http://vlsi-india.org/events/vdat2009/route-map.jpg

Venue Information:
The venue of the Symposium is the Learning center on the Wipro campus, located in Electronic City. To reach the campus, please travel on Hosur road and enter the Electronic City through Phase I gate.

Participants will have to go through Wipro’s Security before entering the campus. Please carry a Government-issued photo-id such as passport or Driver’s license. Please wear the security badge when you are in the campus and return it to the security personnel before leaving the campus.

There are several hotels in Bangalore and information on these is available from the Internet. See the location map shown here. The distance to the venue from Railway station is ~20 km and from the Bangalore International Airport, about 50 km. Due to traffic during morning rush hour and evening rush hour, the actual transit time may be significantly high. Please plan your travel. Weather in Bangalore during August is pleasant, bordering on chilly, with occasional showers.

Speakers will have facilities such as DLP projector, cordless microphone, and whiteboard.

To promote applications and research related to all aspects of VLSI in India.


Regn Entry: Gate 10

Updated: July 13, 2009 - Tutorials | July 9 | July 10 | Committee | Registration | VSI Membership
tutorial – T1  (Participants restricted to 20)  
(Venue: Cranes Software Intl Ltd., # 5, Airport Road, Domlur Layout, Bangalore – 560 071)  
Open Source Embedded System Development using Beagleboard  
Syed Khasim  (Texas Instruments India)

With the availability of low-cost platforms, open-source development of embedded systems is becoming possible for individual hobby professionals and start-ups. In this tutorial, we will introduce the participants to the exciting world of open-source development using the Beagleboard as an example. Beagleboard is intended for low-power, high-performance embedded systems development and supports Linux operating system. A growing world-wide community of Beagleboard users collaborate on solving problems and come up with innovative solutions. In this tutorial, we will cover the following topics and provide some hands-on training on the Beagleboard.

The topics we will cover include:

• Introduction to Open Platforms  
• Quick overview of the Beagle Board  
• Open Software development tools  
• Collaboration tools  
• Validating beagle board peripherals with Linux tools on Beagle Board  
• Introduction to Open Embedded  
• Programming the DSP cores and ARM cores made easy  
• Hands-on Training

Syed Mohammed Khasim started his career back in 2001 with Linux devices for Single board computers and TI DSP applications & solutions. In 2004 he joined Texas Instruments as a Linux Consultant through Wipro technologies. After spending last three years (2004 - 07) in TI head quarters (Dallas, Texas USA) as a Linux Consultant and Open Source Facilitator for Wireless software development & strategies, he moved back to India and joined as a Technical Lead for Open Platforms in DSPS / Catalog applications division of TI. In last couple of years, Khasim has pioneered and lead various initiatives in TI to meet the increase in demand for Mobile Linux on TI chips and processors. Khasim earned a bachelor’s degree in Computer Science & Engg in 2001 from BMS college of Engineering, Bangalore, India.

tutorial – T2  
Compact Modeling and PDK’s  
Madabusi Govindarajan, Tamilmani Ethirajan, Abhisek Dixit, and Josef Watts (IBM)

This tutorial covers compact models and their roles and dependencies in a Process Design Kit (PDK). The emphasis throughout will be to understand the circuit consequences of compact models from an intuitive standpoint. We begin by dissecting a PDK and delve into the mutual dependencies of device views, modelcards, layout-versus-schematic (LVS) decks, and parasitic extraction (PEX) decks. Then we pick up a “simple” device such as a poly resistor and demonstrate how harmonics and self-heating pose modeling challenges for RF front-end designs. Thereafter we escalate the device and model complexity to cover a variety of active and passive device models, culminating in PSP models for ultra deep submicron FET’s. The roles of as-fit and centered models are analyzed in detail. Special emphasis is placed on FET A.C/Noise models and extraction, including the important role of the layout parametric cell-PEX boundary. Statistical modeling is also covered in detail, including Monte Carlo, fixed/functional corners, and statistical timing analysis.

Madabusi Govindarajan received his Bachelor's degree in Electrical Engineering from IIT-Madras in 1988, and the Ph.D degree also in Electrical Engineering from the University of Southern California, Los Angeles, in 1994. At USC he worked on high-speed circuits based on GaAs and InP HBT technologies. From 1994-99 he was a faculty member at the Department of Electrical Engineering, IIT-Bombay, where he became an Associate Professor. At IIT-B Govindarajan taught courses in analog circuits and electromagnetism, and pursued research projects in high-speed systems. From 1999-2002 he worked in the San Francisco Bay Area at LuXn, an innovative start-up in the metropolitan optical networking area. From 2002-05 he was with Scintera, a fabless Bay Area start-up that developed a path-breaking line of 10 Gbps electronic dispersion compensation IC's in standard CMOS. From 2005-2007 Govindarajan was with Signalguru, a Bangalore-based consultancy in high-speed test & measurement. In 2007 he joined IBM’s Semiconductor R&D Center (SRDC) in Bangalore, where he is with the design enablement group, focusing on compact modeling of RF derivative processes. Govindarajan’s technical interests are in high-speed/RF devices and circuits.

Tutorial – T3  
Sarveswara Tammali* (Texas Instruments India)

Test cost is becoming increasingly significant percentage of COB (Cost of Build) in current SoCs (System-on-a-Chip), accentuated by the need of more testing required in shrinking technology nodes. This is even critical in low cost markets like consumer devices. Test quality, which is measured in defective parts per million (DPPM) is becoming aggressive in growing competitive market. So, it is often delicate trade-off that is required to plan test cost strategy given test quality requirements and vice-versa. Strategy includes DFT architecture, target ATE and multi-site configuration and test flow strategy. There are well known DFT techniques namely parallel test, scan compression, built-in-self-test (BIST), which are key techniques in the low cost strategy. Current practices of multi-site test, concurrent tests, scan compression and BIST are discussed. Challenges and impact of these techniques are discussed in detail in this tutorial. The tutorial also talks about some miscellaneous test cost reduction techniques that involve reduction of IDDQ stops and scan pattern optimization. Another important strategy for test cost reduction approach is to use low cost ATE (Automated Test Equipment) as a target tester for SoC. Some of common limitations of low cost ATE are frequency of interaction with DUT, accuracy of stimuli application and output strobe and limited number of tester resources. DFT and test pin muxing, timing closure needs to comprehend limitations of low cost ATE right from design start to be able to successfully utilize low cost ATE for most of tests if not all of manufacturing tests. Key challenges for product engineering team from multi-site point of view are power supply grouping, site-to-site variation, power supply noise and external components on board. In the last section, test cost reduction strategy is discussed which includes test time estimation and identifying critical test modes where test time reduction helps to reduce overall test cost are discussed.

Sarveswara Tammali, IEEe member, obtained an M.Tech in VLSI Design Tools and Technology from IIT Delhi (2001) and joined Texas Instruments India, where he has been responsible for DFT architecture, implementation and support for ramp for several multi-million System-on-a-Chip designs. He has presented several papers in both internal and external international conferences on topics related to Scan Compression, Test Cost Reduction and Failure Analysis. Currently he is actively involved in Test Cost Reduction process. He is also DFT lead for the SOC that has achieved lowest test cost (% of COB) at Texas Instruments and has won best RTP’ed device award with lowest test cost. He has earned his bachelor’s degree in ECE from JNTU College of Engineering, Anantapur, Andhra Pradesh.
**Tutorial – T3**

**Part-II: Test Power Reduction Techniques: Current Practices, Challenges and Impact**

*C.P. Ravikumar and V.R. Devanathan* (Texas Instruments India)

In this part of the tutorial, the speakers will focus on test power reduction. Test power is important from the viewpoint of preventing packaging decisions, device reliability and test effectiveness. The speakers will cover some of the recent techniques for test power reduction, such as hierarchical techniques for power reduction, glitch power reduction, and low-voltage scan shift technique.

C.P. Ravikumar is a senior technologist at TI India. He is also the secretary of the VLSI Society of India since 2003. More details about him can be found at [http://cpravikumar.tripod.com/](http://cpravikumar.tripod.com/)

V.R. Devanathan obtained his B.E. from GCT, Coimbatore, M.Tech. (Computer Science) from IIT Madras, and Ph.D. (Computer Science) from IIT Madras. He has more than six years of industry experience. He is presently with Texas Instruments working on Design for Test related problems for the past five years. He has published papers in the area of Low-Power Testing in leading IEEE conferences and journals. His Ph.D. thesis won the best thesis award at the IEEE VLSI Test Symposium, 2008.

**Tutorial – T4**

**Part-I: Telemedicine**

*Poornima Mohanachandran* (i2i Technologies)

This tutorial will begin by addressing the question of how the medical profession can benefit from technology, in particular, VLSI technology. The tutorial will provide a perspective on the new developments in the area of Tele-Medicine. The tutorial will bring out research & development opportunities and challenges for Indian academia and industry. As an illustration, the topic of medical image compression will be considered and a demonstration will be given of the software developed by an Indian R&D house.

Poornima Mohanachandran has held many executive level management responsibilities at Texas Instruments. She was GM of product development for high performance data converters at Texas Instruments and most recently Director of Business Development for Medical Business at TI. Here she was working with TI customers and medical industry on new opportunities for semiconductor devices in Medical Applications. She has 20 years of industry experience covering all aspects of product development and business development. Presently she is with i2iTeleSolutions a company focused on telemedicine solutions. At i2i she is responsible for strategy and development of telemedicine solutions.

**Part-II: Assistive Devices for the Visually Impaired**

*M Balakrishnan* (IIT Delhi)

In the last three years, an inter-disciplinary group working in the area of embedded systems has been formed at IIT Delhi. The focus of the group has primarily been to design innovative devices for assisting visually impaired persons. In this period we have now worked on four projects that are listed below.

1. Smart Cane
2. Bus identification system
3. Braille tutor
4. Disha: Indoor navigation system

The projects have reached various stages of completion including prototyping and have resulted in one technology transfer done to a company and the second ready for technology transfer. The tutorial would focus on two aspects:

- Technical details and achievements of the four projects and
- A successful model for involving undergraduate students in embedded systems design activity

The tutorial would be accompanied by demonstration of prototypes of these projects. Visit for details - [http://embedded.cse.iitd.ac.in/assistech](http://embedded.cse.iitd.ac.in/assistech)

M Balakrishnan is a professor in the Computer Science Department, IIT Delhi. His research areas include Embedded Systems, CAD for VLSI and Computer Architecture.
# Final Program for July 9, 2009 (Thursday)

<table>
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<tr>
<th>Time</th>
<th>Session</th>
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<td>08.00 AM - 09.00 AM</td>
<td>Registration and Breakfast</td>
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<tr>
<td>09.00 AM - 09.30 AM</td>
<td><strong>Inauguration</strong>&lt;br&gt;<strong>Venue:</strong> Room - Flint</td>
</tr>
<tr>
<td>09.30 AM - 11.00 AM</td>
<td><strong>Session 2A-1: Keynote Talk</strong>&lt;br&gt;<strong>Speaker:</strong> Dr. Biswadip (Bobby) Mitra (President and MD, Texas Instruments India)&lt;br&gt;<strong>Keynote Talk-2</strong>&lt;br&gt;<strong>Embedded Systems: Growing complexity and augmented role of software</strong>&lt;br&gt;<strong>Speaker:</strong> V.R.Venkatesh (Sr. Vice President - Product Engineering Services, Wipro Technologies)&lt;br&gt;<strong>Chair:</strong> TBA&lt;br&gt;<strong>Venue:</strong> Room - Flint</td>
</tr>
<tr>
<td>11.00 AM - 11.30 AM</td>
<td><strong>Tea Break</strong></td>
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</tbody>
</table>
| 11.30 AM - 12.30 PM | **Session 2A-3**<br>**Chair:** K. Radhakrishna Rao (TI India)<br>**Venue:** Room - Flint<br>**A 1.8mW, 320MHz Sigma Delta ADC for Wireless Applications**<br>**Harish Chandraabu** *(IISc Bangalore), and Jamadagni H.S. (CEDT, IISc Bangalore)*<br>108 Regular Paper
| 12.30 PM - 01.30 PM | Lunch                                                                    |
| 01.30 PM - 03.00 PM | **Session 2A-5**<br>**Chair:** N.S. Murty (NXP)<br>**Veriﬁcation**<br>**Relevance of Gate Level Simulations in Today’s SoC Veriﬁcation**<br>**Vishal Dalal** *(SASKEN Communication Technologies Ltd)*<br>42 Short Tutorial
|                  | **Session 2B-5**<br>**Chair:** S.C. Bose (CEERI Pilani)<br>**VLSI in Communication - 2**<br>**Performance Evaluation of an Eﬃcient Boolean Function Generator for Cryptographic Applications**<br>**Debdeep Mukhopadhyay** *(IIT Kharagpur), and Ankur Sharma* *(IIT Madras)*<br>122 Regular Paper
|                  | **Session 2C-5**<br>**Chair:** Dinesh Sharma (IIT B)<br>**VLSI in Biomedical-1**<br>**An Embedded Solution of 2-D Fast Affine Transform for Biomedical Imaging Systems**<br>**Pradyut Biswal**, and **Swapna Banerjee** *(IIT Kharagpur)*<br>51 Regular Paper
|                  | **Process, Temperature, Voltage (PTV) & Load Compensation for IOs**<br>**Vikas Narang** *(Texas Instruments), Nilit Chandrachoodan (IIT Madras), Chennai), and Vinod Menezes (Texas Instruments)*<br>104 Regular Paper
|                  | **Ultra Low Power Digital to Analog Converter**<br>**Raj Dua** *, Sumeet Tiwana, and Anu Gupta (BITS-Pilani)<br>Short Paper 65
|                  | **Virtual Platform for System Integration and Functional Test**<br>**Praveen Kumar** *(NXP Semiconductors India Pvt Ltd)*<br>6 Short Tutorial
|                  | **Addressing Via Density in UDSM Technologies using a Flexible Correct-by-Construction Approach**<br>**Dibyendu Goswami**, Swami Gangadharan, and Albert Holguin *(Intel)*<br>35 Regular Paper
|                  | **Design of Multiple Output, Field Programmable CMOS Voltage Reference Transistors**<br>**Arsh Josan**, Karan Kumar, and Chota Markan *(Dayalbagh Educational Institute, Agra, UP)*<br>118 Regular Paper
|                  | **Design and Analysis of Low Power Viterbi Decoder for CDMA System**<br>**Katki Joshi**, Anand Darji, and Upena Dalal *(SVNIT, Surat)*<br>Short Paper 58
|                  | **Reduced Verification Effort for Low power SoC by using Right Integration, Simulation and QC Strategy**<br>**Mayank Jindal**, Gokulakrishnan Manoharan, Sarveswara Tamnali, and Ayon Dey *(Texas Instruments India)*<br>95 Regular Paper
|                  | **FPGA based Fuzzy Processing System for Advance Detection of Obstructive and Restrictive Pulmonary Disorders**<br>**Shubhajit Roy Chowdhury**, and Hiranmay Saha *(Jadavpur University)*<br>18 Regular Paper
|                  | **Low-Power Adiabatic Flip-flops and Sequential Circuits using ACPL Sreenu D., Ashok Saxena, and Sudeb Dasgupta (IIT Roorkee)*<br>21 Regular Paper
|                  | **A Novel Low Power and High Read Stability SRAM Cell**<br>**Silvamangai N.M.,” Saravanan P., and Gunavathi K (PSG College of Technology)**<br>12 Regular Paper
|                  | **Clock-free Leakage-feedback Gate MTCMOS Flip-flop with a Centralized Sleep switch**<br>**Rahul Singh** *(IT-BHU, Varanasi)*<br>34 Regular Paper
|                  | **Mixed-Clock Interconnect FIFO Design**<br>**Rakesh Yarlagadda**, Jalapally Karthik, and Hemangee Kapoor *(IIT Guwahati)*<br>56 Regular Paper
|                  | **High Speed Leading One Bit Detection based New Scaling Free CORDIC Algorithm**<br>**Supriya Aggarwal**, Kavita Khare, and Nilay Khare *(MANIT)*<br>5 Regular Paper
|                  | **Programmable CMOS Voltage Reference Transistors**<br>**Ashok Saxena, and Sudeb Dasgupta (IIT Roorkee)*<br>21 Regular Paper
|                  | **A Novel Low Power and High Read Stability SRAM Cell**<br>**Silvamangai N.M.,” Saravanan P., and Gunavathi K (PSG College of Technology)**<br>12 Regular Paper
|                  | **Design of Inverse Delayed Function Model of a Neuron for ANN**<br>**Veezhinathan Kamakoti** *(IIT Madras)*<br>18 Regular Paper
|                  | **Design of Multiple Output, Field Programmable CMOS Voltage Reference Transistors**<br>**Arsh Josan**, Karan Kumar, and Chota Markan *(Dayalbagh Educational Institute, Agra, UP)*<br>118 Regular Paper

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**Room Numbers:**
- **Flint:** Ground Floor
- **Quest:** 2nd Floor
- **Amethyst:** Ground Floor
### July 9 Continued

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<tr>
<td>03.00 PM - 03.15 PM</td>
<td>Tea Break</td>
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</tbody>
</table>
| 03.15 PM - 04.30 PM | **Session 2A-6: Panel Discussion**  
Research and Development in VLSI/Embedded Systems  
**Moderator:** C.P. Ravikumar, Texas Instruments India  
**Panelists:** Ramesh N. Raghavan (GM, Wipro Technologies), M. Balakrishnan (IIT Delhi), N.S. Murthy (NXP Semiconductors)  
**Venue:** Room - Flint |
| 04.30 PM - 04.45 PM | **Break**                                                                 |
| 04.45 PM - 05.45 PM | **Session 2A-7**  
Analog VLSI Design - 2  
**Chair:** Swapna Banerjee (IIT KGP)  
**Venue:** Room - Flint  
**Impact of Process Variability on 28nm Analog CMOS Performance**  
Ajayan K. R.*, and Navakanta Bhat  
(IISc, Bangalore)  
Short Paper 57  
**An Alternate Approach to Enhance Parallel Decimal Multiplier Performance**  
Rekha James*, K. Poulouse Jacob  
(CUSAT, Cochi, Kerala), and Sreela Sasi  
(Gannon University)  
4 Regular Paper  
**A High Performance Reference Circuit using Low Input Offset Operational Amplifier**  
Anil Saini, and Kapil Kumar Rajput* (CEERI)  
Short Paper 16  
**An Algorithm for High speed, Low power Implementation of Modular Multiplier**  
Raju Lampande*, Chandrashekar Kukade, Raghvendra D. Deshmukh, and Rajendra Patrikar  
(Visveswaraya National Institute Of Technology, Nagpur)  
Short Paper 99  |
| 04.45 PM - 05.45 PM | **Session 2B-7**  
Digital VLSI Design  
**Chair:** G.S. Visveswaran (IIT D)  
**Venue:** Room - Quest  
**Hardware Implementation of DLighting Module for using it in a Digital Camera Chip**  
Gaurav Agarwal*, Amit Singhal, Anu Gupta, and Prayush Kumar  
(BITS Pilani)  
Short Paper 67  
**Weak Inversion based Low Power Low Noise Sixth order gm-C Filter at 1V for ECG Application with 180nm Technology**  
Anurag Zope*, Waman Khokle, Raghvendra D. Deshmukh, and Rajendra Patrikar  
(Visveswaraya National Institute Of Technology)  
Short Paper 87  |
| 04.45 PM - 05.45 PM | **Session 2C-7**  
VLSI in Biomedical-2  
**Chair:** Shyam Vasudev (Philips)  
**Venue:** Room - Amethyst  
**EEG-based Driving Fatigue Estimation using Discrete Wavelet Transform**  
Sangeeta Panigrahy* (KITS, Warangal)  
Short Paper 116  
**Analysis of Single Event Upset for Biomedical Applications**  
Surendra Rathod*, Ashok Saxena, and Sudeb Dasgupta (IIT Roorkee)  
Short Paper 44  |

**End of Day-2**
### Final Program for July 10, 2009 (Friday) - Day 3

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<th>Time</th>
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<tbody>
<tr>
<td>08.00 AM - 09.30 AM</td>
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<tr>
<th>Time</th>
<th>Session 3A-2 Verification</th>
<th>Session 3B-2 Discussion Meeting with Faculty</th>
<th>Session 3C-2 VLSI Test - 1</th>
</tr>
</thead>
<tbody>
<tr>
<td>09.30 AM - 10.30 AM</td>
<td>Chair: Vineet Sahula (MNIT Jaipur)</td>
<td>Chair: C.P. Ravikumar (TI India)</td>
<td>Chair: Virendra Singh (IISc Bangalore)</td>
</tr>
<tr>
<td></td>
<td>Venue: Room - Flint</td>
<td>Venue: Room - Quest</td>
<td>Venue: Room - Amethyst</td>
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</tbody>
</table>

<table>
<thead>
<tr>
<th>Time</th>
<th>Session 3A-3: Panel Discussion</th>
<th>Session 3B-3: Workshop</th>
<th>Session 3C-3: Poster Session</th>
</tr>
</thead>
<tbody>
<tr>
<td>11.00 AM - 12.00 PM</td>
<td>A Strategy and Framework for Processor Verification</td>
<td>A Novel Test Method for Fault Detection in RF Circuits</td>
<td>Prime Numbers are High Coverage Test Vectors!</td>
</tr>
<tr>
<td></td>
<td>Chair: Vineet Sahula</td>
<td>Chair: C.P. Ravikumar</td>
<td>Chair: Vasantkumar Ramesh</td>
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<tr>
<td></td>
<td>Venue: Room - Flint</td>
<td>(TI India)</td>
<td>(IIT Madras)</td>
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<tr>
<th>Time</th>
<th>Session 3A-4 Research Scholar Forum</th>
<th>Session 3B-4 Low Power Design and Test Session</th>
<th>Session 3C-4 FPGA</th>
</tr>
</thead>
<tbody>
<tr>
<td>12.00 PM - 01.00 PM</td>
<td>Chair: V. Kamakoti (IIT Madras)</td>
<td>Chair: Jais Abraham (AMD)</td>
<td>Chair: V. Kamakoti (IIT Madras)</td>
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<td>Venue: Room - Flint</td>
<td>Venue: Room - Quest</td>
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<tr>
<th>Time</th>
<th>Session 3B-5 Design of Run Time FPGA Router</th>
<th>Session 3C-5 Constructing Synthetic Benchmark Circuits to Stress Test FPGAs</th>
<th>Session 3C-6 Performance Analysis of Low power 6T SRAM Cell in 180nm and 90nm</th>
</tr>
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<tbody>
<tr>
<td>01.00 PM - 02.00 PM</td>
<td>Using JBits 3.0</td>
<td>Using JBits 3.0</td>
<td>Using JBits 3.0</td>
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<td>Haliluz Rahaman (Bengal Engg. &amp; Sc. University), Nachiketa Das (Marine Engineering and Research Institute, Kolkata), and Pranab Roy* (BESUS, Shibpur)</td>
<td>L. Srivani*, Veezhinathan Kamakoti (IIT Madras), and Ilango Sambasivam (IGCAR, Kalpakkam)</td>
<td>Sreeramareddy G.M. (S.V. College of Engg. &amp; Tech., and Ch. Chandrasekarareddy P (JNTUCE, Hyderabad)</td>
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<td></td>
<td>Short Paper 91</td>
<td>Short Paper 90</td>
<td>Short Paper 90</td>
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<tr>
<th>Time</th>
<th>Session 3B-6 Low Power Test Implementation</th>
<th>Session 3C-6 Low Power Test Implementation through Temporal Spreading of Scan Shift/Capture and Q-Gating</th>
</tr>
</thead>
<tbody>
<tr>
<td>02.00 PM - 02.30 PM</td>
<td>Through Temporal Spreading of Scan Shift/Capture and Q-Gating</td>
<td>Through Temporal Spreading of Scan Shift/Capture and Q-Gating</td>
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<td>Pranay Kotasthane, Sreefsha Arisetti, Sreeram Chandrashanker, Kishore Kumar Robbi*, and Anirban Saha (Texas Instruments India)</td>
<td>Pranay Kotasthane, Sreefsha Arisetti, Sreeram Chandrashanker, Kishore Kumar Robbi*, and Anirban Saha (Texas Instruments India)</td>
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<tr>
<th>Time</th>
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<tbody>
<tr>
<td>01.00 PM - 02.00 PM</td>
<td>Lunch</td>
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**Notes:**
- VMM Methodology Template Code Generator
- A Strategy and Framework for Processor Verification
- Simulation-less Point-to-Point Connectivity Checks for SOC Environment
- A High Performance Implementation of LU Decomposition on FPGA
- Design of Run Time FPGA Router using JBits 3.0
- Constructing Synthetic Benchmark Circuits to Stress Test FPGAs
- Performance Analysis of Low power 6T SRAM Cell in 180nm and 90nm

**Additional Information:**
- VLSI Society of India will host a meeting of faculty and industry professionals to discuss curriculum related issues.
- Prime Numbers are High Coverage Test Vectors!
- Low Power Test Implementation through Temporal Spreading of Scan Shift/Capture and Q-Gating
- The Final Program for July 10, 2009 (Friday) - Day 3 concludes at 02.30 PM.
### Session 3C-5
**Design Automation**
**Chair:** C.P.Ravikumar (TI India)  
**Venue:** Room - Flint

#### How to Accommodate Design Changes using Standard Cell Library
Radhika V. Guttal, Harish Venkatesh, and Akhtar W. Alam (ARM Embedded Technologies)  
Invited talk

#### Uniform Thermal Distributions in Placement of Standard Cells and Gate Arrays: Algorithms and Results
Prasun Ghosal*, Hafizur Rahaman (Bengal Engineering & Science University), and Partha Dasgupta (IIM Calcutta)  
Short Paper 72

#### Surface Potential Based Current Modeling of Thin Silicon Channel Double and Tri-Gate SOI FinFETs
Robin Prakash*, Rohit Yadav (BITS, Pilani), and Subhash Bose (Central Electronics Engineering Research Institute, Pilani)  
20 Short Paper

#### Simulation of Improved Dynamic Response in Active Power Factor Correction Converters
Matada Mahesh*, and Anup Kumar Panda (NIT Rourkela)  
Short Paper 77

### Session 3B-5
**VLSI Test - 2**
**Chair:** Adit Singh (Auburn Univ.)  
**Venue:** Room - Amethyst

#### BIST / Test-Decompressor Design using Combinational Test Spectrum
Nitin Yogi, and Vishwani Agrawal* (Auburn University)  
82 Regular Paper

#### Synthesis of Analog Inputs for Testing of Digital Modules in Mixed Signal VLSI Circuits
Chiranjeevi Yarra* (IIT, Kharagpur), Santosh Biswas (IIT, Guwahati), and Siddarth Mukhopadhyay (IIT, Kharagpur)  
63 Short Paper

#### Performance Evaluation of Mesh-of-Tree Based Network-on-Chip Using Wormhole Router with Poisson Distributed Traffic
Santanu Kundu (IIT Kharagpur), Radha Purnima Dasari * (Texas Instruments, Bangalore), Kanchan Manna, and Santanu Chattopadhyay (IIT Kharagpur)  
Short Paper 61

### Research Scholar Forum
**Continued**

### 03.45 PM - 04.45 PM

### Session 3A-6
**Valedictory**
**Chair:**  
**Venue:** Room - Flint

### End of Symposium
**VDAT2009 Symposium Committee**

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vsiaccount@vlsi-india.org

| Registration Information: |
| Registration permits you to participate in all the Technical sessions and Tutorials organized as part of the Symposium, and includes refreshments and lunch on all days. |
| Tutorials and Symposium needs separate registration. A common payment for both is preferred. If applying separately, please repeat the registration process for each. |
| Please send your registration fee through a draft made out to VDAT Symposium 2009, payable at Bangalore. Follow the before/ after deadline rate. If the DD is made out on or before the deadline, and reaches us slightly late, it would be considered as before-deadline. |
| The draft must be sent to Mr. Gopal Naidu, Finance Chair (VDAT 2009), Texas Instruments India, Bagmane Tech Park, C.V. Raman Nagar, Bangalore 560093. |
| If you wish to register on the spot, drafts and cash payment in Indian rupees are acceptable. We will not be able to accept Credit Card payments. |
| The current exchange rate is approximately 1 US dollar = 50 Indian rupees. |
| Even those of you who plan to register on the spot are requested to communicate your desire to attend VDAT 2009 through online form. Details of vehicle registration (if any) and laptop number (if any) should be sent to vdat-local@vlsi-india.org with a copy to vdat@vlsi-india.org. Without this, you may face difficulties during registration. |
| If you are registering for a tutorial, indicate the first and second preference of the tutorial. There are limited seats in each tutorial. If we cannot register you in the tutorial of your choice, we will refund the amount. |
| A processing fee of Rs 500/- will be applied against all cancellations. |
| Bulk Registration: We will offer one complimentary registration for every five registrations received from the same organization. All the six names should be registered with full information quoting the same DD details. Authors of accepted papers may also be included. |

**Members of VLSI Society of India or IEEE get discounted rates**

<table>
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<tr>
<th><strong>Tutorial Registration Amount</strong> (July 8, 2009)</th>
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<td><strong>Before June 22, 2009</strong></td>
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<td><strong>Category</strong></td>
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<td>Students</td>
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<tr>
<td>Faculty Members and Government R&amp;D</td>
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<td>Indian Industry Participants</td>
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<table>
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<tr>
<th><strong>Symposium Registration Amount</strong> (July 9-10, 2009)</th>
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<td>Indian Industry Participants</td>
</tr>
<tr>
<td>Foreign Participants</td>
</tr>
</tbody>
</table>

Please carry the following with you:

- Government-issued ID card such as passport/Driver’s license
- Student ID card (for student participants)
- You will be required to provide your contact phone number and address at the security booth.

Entry for VDAT is from Gate 10 of Wipro Campus, EC Phase 4. Please send a mail to vdat-local@vlsi-india.org (with a copy to vdat@vlsi-india.org) and inform your vehicle’s registration number and Laptop number if you will come in your private vehicle and/or bring your laptop.

**History of VDAT:**

<table>
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<th>Event Title</th>
<th>Venue</th>
<th>Date</th>
<th>Participants</th>
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<td>January 7, 1998</td>
<td>30</td>
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<tr>
<td>2nd VDAT</td>
<td>New Delhi</td>
<td>August 6-7, 1998</td>
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<td>3rd VDAT</td>
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# REGISTRATION FORM

**Name of the participant:** (Please use block letters.)

<table>
<thead>
<tr>
<th>Category (Tick appropriate)</th>
<th>Student</th>
<th>Indian academia/ Government R&amp;D</th>
<th>Indian Industry</th>
<th>Foreign Participant</th>
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<tr>
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<td>Member</td>
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**Student ID/ Register No:**

**VSI/ IEEE Membership No:**

**Indian academia/ Government R&D**

**VSI/ IEEE Membership No:**

**Indian Industry**

**VSI/ IEEE Membership No:**

**Foreign Participant**

**Address for Correspondence**

**Designation**

**College/ Company Name**

**Permanent address:**

**E-mail** (Compulsory):

**Choice of tutorial:** T1  T2  T3  T4

**Payment Details**

<table>
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<th>Towards Tutorial</th>
<th>Towards Symposium</th>
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<td>DD Number</td>
<td>Dated</td>
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**Total Amount**

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Which days do you wish to attend? (Tick appropriate)

- T1 only
- T2 only
- T3 only
- T4 only
- Symposium only
- Symposium + T1
- Symposium + T2
- Symposium + T3
- Symposium + T4

**E-mail**

**Telephone:**

**Signature**

**Tutorial Registration Amount**

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<td>Government R&amp;D</td>
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<td>Indian Industry</td>
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<td>Foreign Participants</td>
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<td>USD 75</td>
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**Symposium Registration Amount**

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<td>Foreign Participants</td>
<td>USD 75</td>
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<td>USD 100</td>
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**Note:**

- **Symposium registration fee includes registration material, lunch and refreshments on all the days.**
- **If registering separately for Symposium and Tutorial, please submit separate forms for each. Transport and stay arrangements are the responsibility of the participants.**

**VLSI** indicates VLSI Society of India or IEEE member

**Mail the completed registration form and DD to the following address:**

- Mr. Gopal Naidu
  - Treasurer, VLSI Society of India
  - Finance Department
  - Texas Instruments (India) Pvt Ltd
  - Bagmane Tech Park
  - C.V. Raman Nagar, Bangalore 560093
  - Phone: 080-2509 9363
  - FAX: 2509 9717
  - vsiacounts@vlsi-india.org

**Important Notes:**

- The DD to be made out to “VDAT Symposium 2009” payable at Bangalore, India. On the rear side of DD, please write Towards VDAT2009 (Symposium/Tutorial/Symposium+Tutorial).
- The DD and form to be sent to the VDAT2009 Finance Chair, to Bangalore address mentioned on the left.
- You must also enter the above details electronically at http://vlsi-india.org/register.htm to receive information from us regularly
- Queries regarding registration must be sent only to: vsiacounts@vlsi-india.org with a copy to vdat@vlsi-india.org
- Students should send a photocopy of the ID issued by the college along with the registration form.
- **Bulk Registration:** We will offer one complimentary registration for every five registrations received from the same organization. All the six names should be registered with information quoting the same DD details. Authors of accepted papers may also be included.

**Please watch the VDAT website or follow the vdat@yahoogroups.com mailing list for any updates to the program. Since the space for tutorials is limited, we may be forced to shortlist participants. If we are unable to register you, you will be intimated by e-mail, and a refund will be made by the VLSI Society of India. Watch VDAT2009 website for general updates.**
# VSI Membership Form

**VLSI Society of India**

http://vlsi-india.org/vsi/

Registered Society under KSR Act 1960, Rule 1961

E-mail: vsiaccounts@vlsi-india.org, vsisecy@vlsi-india.org

1. **Existing Membership No:**
   (Quote additional Old No. If any):

2. **Your Name:**

3. **Your Profession/Designation:**

4. **Your e-mail address:**

5. **Your Contact address:**

6. **Your Professional address (if different from above):**

7. **Your Area of specialization:**

8. **Would you like to review papers in events organized by VSI?**

9. **How many papers are you willing to review?**

10. **Your Brief bio-data:** Attach separately

11. **How can you contribute to the activities of VSI?**

12. **What Activities would you like VSI to organize?**

13. **Details of Payment:**

<table>
<thead>
<tr>
<th>Category</th>
<th>Membership Rates:</th>
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</thead>
<tbody>
<tr>
<td></td>
<td>Yearly</td>
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<tr>
<td>Student Member</td>
<td>Rs. 500/=</td>
</tr>
<tr>
<td>Non-student member</td>
<td>Rs. 1,000/=</td>
</tr>
<tr>
<td>Corporate member</td>
<td>Rs. 10,000/=</td>
</tr>
</tbody>
</table>

Mail the form along with the DD to:

Mr. S.R. Gopal Naidu, Treasurer VSI
Texas Instruments India Pvt. Ltd
Bagmane Tech Park, Adjacent to LRDE, C.V. Raman Nagar
Bangalore: 560 093 (FAX: 91-80-25048213)

The DD to be made out to: "VLSI Society of India" and payable at Bangalore.

- Please also enter the details in the online membership form http://vlsi-india.org/vsi/activities/reg.shtml to update records.
- Processing the card subject to the DD receipt. Please allow two weeks.
- The photograph is for official records only and will not be imaged onto the membership card.
- Inscribe "Towards VSI Membership - New/ Renewal" at the rear side of DD. Students to attach college credentials.
- The same form to be used for a new membership or Renewal. In the event of change of address, please update online.
- Please do not send scanned images of DD or the Form. Processing the card subject to the DD receipt. Allow two weeks.
- Become a VDAT Yahoogroup member to receive updates on all announcements. Details on http://vlsi-india.org/docs/mailgroup.shtml

**Place and Date:**

<table>
<thead>
<tr>
<th>Membership No.</th>
<th>Signature</th>
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I agree to be a member of the VLSI Society of India and have read and understood the charter of the society.

I will actively contribute towards the objectives of the society.

**Recommended by VSI Members:**

<table>
<thead>
<tr>
<th>Name</th>
<th>Membership No.</th>
<th>Signature</th>
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