Updated: 11 June 2008

The objective of TI's University Analog Program is to introduce cutting edge Analog technology into Indian academia through focused and targeted training.

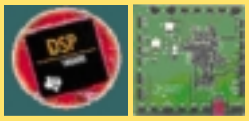
The participants are faculty from selected colleges across India.

The goal of this three-day workshop is to expose faculty to *system-level design* using TI DSP, TI Microcontrollers, Data Converters, and Audio Codecs. The course will include lecture classes, demonstrations, and hands-on.

Faculty who will take part in this program will carry back with them a unique experience in system design and interfacing analog subsystems to the digital processor.

TI India University Analog Program

Three-day Workshop on Audio Codecs and Data Converters



June 16-18, 2008
Venue: Jadavpur University, WB, India
Sponsored by
Texas Instruments India
Tata Consultancy Services
Supported by
Jadavpur University and **VLSI Society of India**
Technical Sponsor
IEEE Calcutta Section

VLSI Society of India

যাদবপুর বিশ্ববিদ্যালয়

Dr. Bobby Mitra, M.D. Texas Instruments India

Texas Instruments India is proud to support the University Analog Program. The program has a noble and very important goal of bridging the gap between the Universities and Industry. I am excited about the program being planned in Jadavpur University during the summer of 2008: System Design and Analog Interfacing – a topic that even experts acknowledge as a major challenge! As a world leader in Analog, DSP, and Microcontroller products, TI is keen to support the growth system design competency in India. I am sure both the faculty and TI India professionals will benefit from this unique interaction!

Workshop Committee

C.P. Ravikumar, TI India	Coordinator
S K Sanyal, Jadavpur University	Coordinator
Supriyo Palit, TI India	Coordinator
K. Radhakrishna Rao, TI India	
Poornima Mohanachandran, TI India	
S. Janakiraman, TI India	
Anand K, TI India	
Uttam Agarwal, TI India	
S.K.Sandeep, TI India	
Gaurav Jain, TI India	

Program Schedule

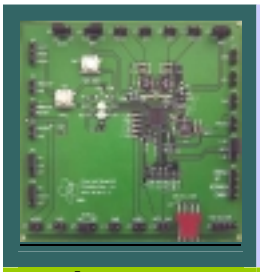
Participants must report to the registration desk on June 16-18 at 8.45 AM. Participants must make their travel arrangements accordingly. The morning tutorial session begins at 9.30 AM and concludes at 1.00 PM on all days. The afternoon lab session begins at 2.00 PM and concludes at 5.15 PM on all days. There will be a lunch break (1.00 PM – 2.00 PM) and two coffee breaks (11.00 AM – 11.30 AM and 3.30 PM – 4.15 PM) on all days.

On the first day, a brief inauguration ceremony is planned. Certificates of participation will be distributed in the valedictory function planned on the last day. Participants must ensure that they are present to collect their certificates. Course notes/handouts will be made available on a daily basis. Discussions on curriculum are planned during the course and selected faculty will be requested to make short presentations on the current curriculum.

Advanced Technical Program: June 16 – 18, 2008

	Morning (9.30 AM – 1.00 PM) Venue – Vivekananda Hall, Raja S. C. Mallik Road, JU		Afternoon (2.00 PM – 5.00 PM) Venue – Networking Lab	
Day 1	09.00 AM – 9.30 AM	**Registration**	02.00 PM – 4.00 PM	Introduction to TI Ultra low-power Microcontroller MSP430 **(Gurjit Singh Gill, Gill Instruments)**
	09.30 AM – 10.00 AM	**Inauguration**	04.30 PM – 5.30 PM	Introduction to Analog Lab-in-a-box **(Gaurav Jain)**
	10.00 AM – 11.00 AM	A perspective on Analog System Design **(K.Radhakrishna Rao)**	05.30 PM – 6.30 PM	Hands-on Lab on TI TINA **(Sandeep SK)**
	11.30 AM – 12.30 AM	Exploring the SPICE Simulator – TI TINA **(SK Sandeep)**		
Day 2	09.30 AM – 10.00 AM	Introduction to TI Analog Products (Anand K)	02.00 PM – 05.00 PM	Demo of applications on Codec EVM (Uttam Agarwal)
	10.00 AM – 11.30 AM	Introduction to Audio Codec ICs (Anand K)	05.00 PM – 5.30 PM	Case Study of Interactive Set Top Box developed by TCS on TI Da Vinci platform (Debnarayan Kar, TCS)
	12.00 Noon – 1.00 PM	Introduction to Codec EVM (Uttam Agarwal)		
Day 3	09.30 AM – 10.30 AM	Introduction to TI DSP Kits **(Vinod Geo Thomas)**	02.00 PM – 3.00 PM	Demonstration of System Design Experiments **(Supriyo Palit)**
	10.30 AM – 11.30 AM	Interfacing DSP with Audio Kits **(Supriyo Palit)**	03.00 PM – 3.30 PM	Analog/System Curricula in Universities - Participating faculty **(Poornima)**
	12.00 AM – 1.00 PM	Interfacing DSP with Audio Kits **(Supriyo Palit)**	04.00 PM – 4.30 PM	Workshop feedback and future plans **(Poornima)**
			04.30 PM – 5.00 PM	Distribution of certificates **(Poornima)**

Please also register online at http://vlsi-india.org/vsi/activities/reg.shtml apart from sending the filled hardcopy of registration form.

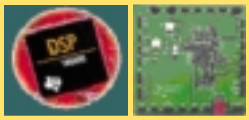


ABOUT THE FACULTY

Faculty	Profile
K. Radhakrishna Rao 	**K. Radhakrishna Rao** is a Distinguished Member of Technical Staff (Emeritus) at TI India. He was with the Department of Electrical Engineering, IIT Madras, during 1971-2006 before he joined TI India. He obtained his Ph.D. (EE) from IIT Kanpur (1971) and B.Tech (EE) from IIT Madras (1966). His current interests are in analog IC design and continuous-time filters. He has taught Analog 101 (Introduction to Analog IC Design) and Analog 203 (Analog Filters) in PragaTI. **Contact:** krkrao@ti.com
Supriyo Palit 	**Supriyo Palit** is an applications engineer in TI India. His professional experience includes 11 years in the area of speech/audio/video processing, wireless communications and networking, TI processors, and TI analog codecs. Supriyo has an M.E. in Electrical Communications Engineering. His current interest is Audio Signal Processing. He has taught courses on digital filter design and Bluetooth systems in PragaTI. **Contact:** riyo@ti.com
Debnarayan Kar	**Debnarayan Kar** received his Bachelor of Engineering degree in Computer Science & Engineering in 1995 from National Institute of Technology (formerly REC) Durgapur. After that he worked in UBEST until 1998 where he worked to develop Billing and Mediation software for cellular telecom operators. From 1998 to 2000 he worked in the development team of enterprise network management software Unicenter TNG in Computer Associates TCG Software (CATS). Between 2000 and 2007 he was part of the R & D team of Marconi and Ericsson for their cellular network planning & optimisation solution Planet DMS and Planet EV. During this tenure he contributed to bring out some of the major releases of Planet DMS and Planet EV which where accepted by more than 130 customers globally. Since January 2007 he is in TCS where is primarily focussing on customer projects and R & D initiative in wireless telecommunication and multimedia areas.
Gaurav Jain	**Gaurav Jain** works for Texas Instruments India.

Faculty	Profile
Anand K 	**Anand K** is a lead engineer at TI India. He is a member of Group, Technical Staff in TI Tech Ladder. He has been with TI India since 1996. Anand obtained his MSc (Engg) from IISc Bangalore in 1996 and a B.Tech in Electrical Engineering from IIT Madras in 1993. His current interests include Analog IC design, Data Converters, and Low Power Audio IC design. He was part of the faculty team, which has taught Analog 101 (Introduction to Analog IC Design) in TI India Technical University. **Contact:** anandk@ti.com
Gurjit Singh Gill	Gurjit Singh Gill is the Director /Design Head, at Gill Instruments Bangalore, a third-party company of Texas Instruments. He has 7 years of work experience in the field of embedded systems. His has worked as an Embedded Design Engineer for G.E Power controls Bangalore, and also at Bajaj Auto, Garware Polyester, and Cosmo films; Everest Kento Cylinders, Vatan Textile, and Jacob Muller (India) Pvt. Ltd. He presented a keynote speech, *Embedded system design using MSP430* and conducted tutorials on *Single chip Filter*, at the Texas Instruments Developer conference during 2004-2005. He has worked on wireless Acoustic sensors using MSP430 for Fire Alarm system, implementing Filter algorithm and echo cancellation techniques. He has designed one of the first development tools to support Acoustic sensor interface that employed the on board microphone and low power amplifier with wire/wireless interface. Currently he is working on TCP/ IP, USB and wireless protocols.
Uttam Agarwal 	**Uttam Agarwal** is part of the Mixed Signal Technology Center (Audio) group in Texas Instruments, Bangalore, India. He has conducted several training programs based on TI audio products for both customers and for universities. **Contact:** uka@ti.com
Vinod G. Thomas 	**Vinod Geo Thomas** is a Senior Software Engineer at Cranes Software International Ltd. He completed his M.Tech in Telematics & Signal Processing from NIT (Rourkela). His focus area is speech/audio algorithms on TMS320C6000 architectures. In his professional experience of over 5 years, he has conducted numerous trainings on TI processors and speech applications for corporates and academia.
Sandeep SK 	**Sandeep SK** has a B.Tech. in Electronics and Communication Engineering from NIT (formerly REC) Calicut. He is with TI India since 2004. His interest is in Analog EDA. He has conducted training programs on SPICE simulation.

TI India University Analog Program
Three-day Workshop on
Audio Codecs and Data Converters



June 16-18, 2008 - Venue: Jadavpur University, WB, India

REGISTRATION FORM

Name of the participant:

(Please use block letters. The participation certificate will be made in this name)

Please let us know which TI products you already use in your labs (DSP kits, MSP kits, Analog kits)

Please summarize the benefits you will be able to get from attending this program. In particular, tell us if you can modify your existing lab curriculum, theory course curriculum, add a new lab, or add a new theory course in the area of Analog Subsytem Design/Analog Interfacing/System-level Design. Please use a separate sheet.

Contact Address: (Provide the address of your college and the permanent mailing address)	**College Address:** **Preferred Mailing address (if different from above):**

E-mail:		**IEEE/ VSI/IETE** Regn no.	

Background in Analog Design: Please provide a brief professional history, starting from your present position and going back in reverse chronological order. Please list what courses (PG/UG) you teach in Analog Design, any professional courses you have undergone and any papers you may have published.	
Would you like to make a presentation about the curriculum in Analog Design/System design at your institution?	(If yes, please plan for a 10-minute presentation and discussion on Day 1.)
Would you like accommodation in Jadavpur University Gueshouse? You are expected to make your own travel arrangements.)	A limited number of rooms may be available for participants. We can block the rooms if you inform us before **May 20, 2008**. The charges towards accommodation are Rs 400/ day. Guests are expected to clear the dues directly at the counter.

Registration Charges
(The cheque/DD to be made out to **VLSI Society of India**, payable at Bangalore)
Outstation cheques should include necessary bank charges.

Last date to receive registration: May 31, 2008		
Category	**Members of IEEE/VSI/IETE**	**Non-members**
Faculty	Rs 1000/-	Rs 1500/-
Industry Professionals	Rs 3000/-	Rs 3500/-
Research Scholars	Rs 800/-	Rs 1000/-

Your expectations from the workshop:

I have/will be able to obtain the approval from my organization to attend the workshop.
I will make my own travel arrangements.

Signature

Mail the completed registration form to the following address:

S.R.Gopal Naidu
Trasurer, VLSI Society of India
Texas Instruments India
Bagmane Tech Park
CV Raman Nagar
Bangalore 560093
vsiaccounts@vlsi-india.org

Also, please register online at
http://vlsi-india.org/vsi/activities/reg.shtml

- Invitation cannot be transferred to another colleague.
- You must attend the entire workshop.
- Please let us know immediately if you have any difficulty in attending the program, so that we can operate the waiting list.
- The cheque/DD to be made out to **VLSI Society of India**, payable at Bangalore
- Please inscribe **"TI India University Analog Program – Jadavpur University"** at the rear side of the chq/DD.
- For outstation cheques, please add the required Bank charges.

Note:	All participants will receive registration material, lunch and refreshments on all the days. Participants are expected to make their own travel arrangements. Guesthouse accommodation in Jadavpur University will be available against a payment to those who have informed the committee in advance.