

# Choosing Data Acquisition Boards and Software

*Data Translation manufactures data acquisition boards and software for use in a variety of computers. This includes the DT300, DT3000, and DT3010 Series for the PCI bus, and the PC Card-EZ,<sup>™</sup> DataAcq-EZ,<sup>™</sup> DT2801 Series, DT2821 Series, DT2831 Series, and DT3831 Series for IBM<sup>®</sup> PC compatibles.*



*PCI-EZ brings high-performance data acquisition to the PCI Bus.*

## The Basics—Analog-to-Digital (A/D) Conversion, Digital-to-Analog (D/A) Conversion and Digital I/O

Data acquisition boards help you measure real-world information represented by analog signals. The analog signals come from sensors or transducers that convert temperature, pressure, sound, or light into voltage. The electronic sampling of analog signals is called A/D conversion or analog-to-digital conversion. A/D conversion changes real-world analog voltages into digital codes for computer processing and storage.

A complementary process, D/A conversion (digital-to-analog conversion) changes digital data into analog voltages. This permits a computer to drive chart recorders, audio amplifiers, process actuators, and other devices requiring an analog driving voltage.

Many data acquisition boards have both A/D and D/A converters. These permit computerized measurement and control of industrial processes and lab experiments, or recording and playback of audio signals.

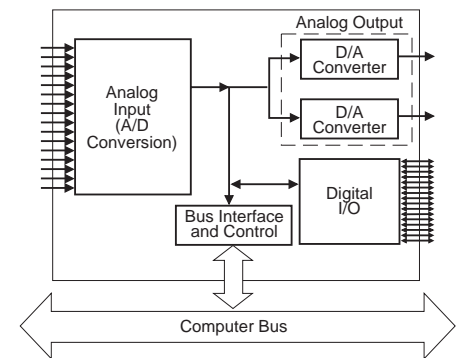
To communicate with a device that itself is digital, many data acquisition

boards provide digital I/O (digital input/output or DIO) lines. Digital I/O lines can be set for input or output operation in groups called ports, often composed of eight lines.

## Input Ranges (Unipolar, Bipolar, PGH, PGL, Channel-Gain List)

One of the first things to consider in choosing a data acquisition system is the voltage range to measure. Begin by picking the type of sensor or sensors you will use—strain gauge, thermocouple, microphone, or pressure transducer, for example. Then determine the range of output voltages this sensor will provide (the sensor manufacturer can supply this information).

Input ranges for data acquisition boards are listed in each data sheet. Ranges can be unipolar (0-10 V, for example, for positive voltages only) or bipolar ( $\pm 10$  V, for example, for both positive and negative voltages). Pick a board that covers the range you wish to measure with as little overlap as possible. This will give you the greatest number of data points in the range you



*Multifunction data acquisition board with analog input, analog output, and digital I/O subsystems.*

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## Programmable Gain and Input Ranges

	High-Level Gains (PGH)				Low-Level Gains (PGL)			
	1	2	4	8	1	10	100	500
Unipolar	0-10 V	0-5 V	0-2.5 V	0-1.25 V	0-10 V	0-1 V	0-.1 V	0-.02 V
Bipolar	$\pm 10$ V	$\pm 5$ V	$\pm 2.5$ V	$\pm 1.25$ V	$\pm 10$ V	$\pm 1$ V	$\pm .1$ V	$\pm .02$ V

Channel-Gain List

Entry	Channel	Gain
0	1	1
1	7	2
2	4	1
3	10	4
4	1	2
5	12	1
6	9	8
7	11	1

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This channel-gain list samples channels in any sequence you specify at any available gain. You can even sample the same channel (channel one) at different gains.

wish to measure, and so the highest accuracy. For example, if the sensor output varies from 1 to 3 V, choose a board with a 0-5 V range. This will give you twice as many valid data points, or twice as much resolution, as an input range of  $\pm 5$  V or 0-10V, since the counts for ranges  $-5$  V to 0 V and for  $+5$  V to  $+10$  V would not be used. A lower voltage range (0-2.5V, for example) would not let you measure the full output of the sensor.

Most data acquisition boards (such as the DT3010, DT300 Series, DT01-EZ, DT21-EZ Series, DT31-EZ, and most DT2821 and DT2831 Series models), provide multiple input ranges by using software-programmable gain amplifiers. Data Translation offers high-level programmable gain (PGH) models, which provide gains of 1, 2, 4, and 8 and can measure inputs as low as 1.25 V with full resolution; and low-level programmable gain (PGL) models that provide gains of 1, 10, 100, and 500 and can measure signals as small as 20 mV with full resolution.

While programmable gain lets you change the input range in software, it has one disadvantage: changing the gain requires an extra software instruction,

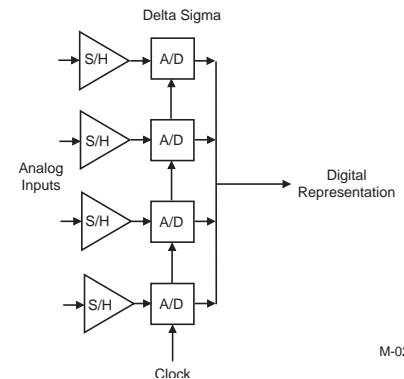
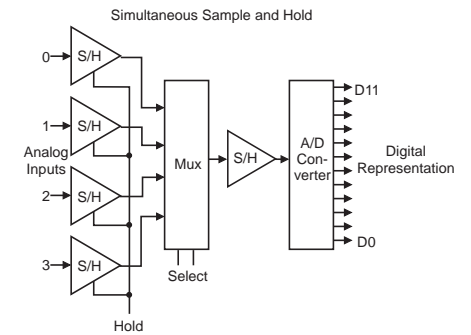
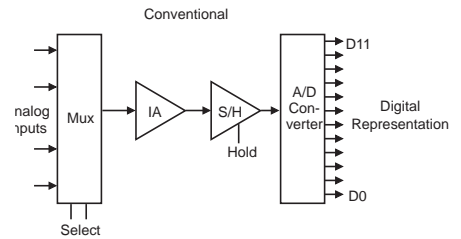
which can slow high speed data acquisition. The channel-gain list, a feature on many Data Translation high-performance boards (such as the DT300 Series, DT3010, DT21-EZ Series, DT31-EZ, DT2821 Series, and DT2831 Series), provides an elegant solution. The list, actually a small onboard memory buffer, is preloaded with up to 32,768 channel numbers and associated gains. During data acquisition, the channel-gain list automatically selects channel and gain values in hardware without compromising throughput.

**Input Types (Channels, SE/DI, Pseudo-Differential, CMRR, Simultaneous Sampling)**

The number of input channels available determines the number of devices you can connect to an A/D board. The number of channels ranges from 4 to as many as 64. However, accessory products like the DT2896 Channel Expander for the DT2839 and the DT727 Channel Expansion Panel permit a compatible A/D board to sample up to 256 inputs (data sheets indicate which products are compatible with the DT727).

Input channels can be single-ended (SE) or differential (DI), a characteristic you can set on many data acquisition boards. Data sheets present this as "16SE/8DI," meaning you can set the board for 16 single-ended or 8 differential inputs.

Since you get half as many differential inputs as single-ended, why would you ever choose differential? Differential inputs offer a kind of noise immunity called common-mode rejection, abbreviated as CMRR (common mode rejection ratio), and given in decibels or dB. As the name suggests, differential inputs respond mainly to the differences in voltage levels between the two signal leads, and can improve accuracy where long



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Conventional data acquisition systems have a single sample and hold circuit, and sample inputs sequentially. Simultaneous Sample and Hold systems have one sample and hold input for each input, and can thus freeze values on all inputs simultaneously. Delta-sigma designs use a separate A/D converter per channel, and can both simultaneously sample and convert data values on all channels.

cables, low-level input ranges (<1 V full-scale), or high-resolution converters (>16 bits) are used. Differential inputs are also recommended where input signals from different devices are at different ground potentials—differential inputs can float several volts with respect to one another, to analog ground, and to power ground.

## Using Low-Pass Filters to Eliminate Sampling Errors in A/D Conversion Systems

### The Aliasing Phenomenon

Everyone who has gone to the movies has probably seen an example of aliasing. It's what makes the spokes of a wagon wheel or the rotor blades of a helicopter appear to be rotating slowly backwards.

In data acquisition systems, aliasing is a sampling phenomenon that can cause gross errors in results and reduce the accuracy of the data collected by an A/D board, which converts the analog output of a sensor into a digital number that can be read by the acquisition system's computer. It occurs whenever an input signal has frequency components at or higher than half the sampling rate. If the signal is not correctly band limited to eliminate these frequencies, aliases or spurious lower frequency errors occur which cannot be distinguished from valid sampled data. The alias signals are actually at a higher frequency, but are converted by the sampling process to a false frequency below half the sampling rate. For example, with a sampling rate of 1,000 Hz, a signal at 800 Hz aliased to 200 Hz (the false lower frequency). Thus, aliasing is a phenomenon that occurs when a high-frequency component effectively takes on the identity of a lower frequency.

One solution to the aliasing problem is to sample the signal at a very high rate and then filter out the high frequencies with digital techniques. But, such oversampling of data increases system costs by requiring faster A/D conversion for digital processing, more memory, and higher bandwidth buses. It also leads to higher analysis costs by creating more data to process and interpret.

### Low-Pass Filtering

A more practical alternative is to limit the bandwidth of the signal below one-half the sample rate with an anti-alias filter, which can be implemented on

each input channel in front of the A/D converter. Anti-alias filtering must be done before the signal is sampled or multiplexed, since there is no way to retrieve the original signal once it has been digitized and aliased signals have been created.

To avoid aliasing with a low-pass (or anti-aliasing) filter, two processes actually must occur:

- As dictated by the Nyquist theory, the input signal must be sampled at a rate of at least twice the highest frequency component of interest within the input signal.
- Any frequency components above half the sampling rate (also called the Nyquist frequency) must be eliminated by an anti-alias filter before sampling.

Under ideal conditions, a low-pass filter would exactly pass unchanged all slower signal components with frequencies from DC to the filter cutoff frequency. Faster components above that point would be totally eliminated, reducing the signal disturbance. But, real filters do not cut off sharply at an exact point. Instead, they gradually eliminate frequency components and exhibit a falloff or rolloff slope.

### Filter Types

Among the types of filters more commonly used for anti-alias purposes are Cauer (Elliptic) filters, Bessel filters, and Butterworth filters. No filter is perfect, and different types of filters are imperfect in different ways. The optimum filter type for an application depends on which kinds of imperfections are most easily tolerated. Examples of imperfections include phase non-linearity, gain error, passband ripple and droop, and wideband noise.

An extremely sharp cutoff-frequency rolloff makes Cauer filters ideally suited for most anti-alias applications. Cauer

filters also have good passband flatness and low wideband noise. But, their non-uniform group delay can cause some overshoot or ringing in time-domain plots if the input signal has sharp transitions. Bessel filters, on the other hand, have a uniform group delay with no ringing or overshoot. They are best suited for time-domain anti-alias applications requiring minimum distortion of rapid slope changes. Butterworth filters are useful when maximum passband flatness is critical. Both Bessel filters and Butterworth filters have a gentler cutoff slope as compared to the Cauer.

### Summary

The aliasing phenomenon becomes a problem in A/D conversion systems when an input signal contains frequency components above half the A/D sampling rate. These higher frequencies can "fold over" into the lower frequency spectrum and appear as erroneous signals that cannot be distinguished from valid sampled data. The best approach to eliminating false lower frequencies is to use a low-pass filter, which inhibits aliasing by limiting the input signal bandwidth to below half the sampling rate.

### Benefits of Using Low-Pass Filters

Applied to each input channel in front of the A/D board, a low-pass filter can eliminate high-frequency noise and interference introduced prior to sampling. It can reduce system cost, acquisition storage requirements, and analysis time by allowing for a lower sampling rate. A low-pass filter also can serve as an important element of any data acquisition system in which the accuracy of the acquired data is essential.

A third type of input, known as pseudo-differential, gives enhanced common-mode rejection in designs where there is not enough space or power for true differential input circuitry (as is the case with the DT7101 and DT7102). This design provides connections for both the low end and the high end of each input to achieve improved analog common-mode rejection. However, unlike true differential, only one of the signals is actually sampled by the A/D converter.

Some applications, such as destructive testing, involve the simultaneous sampling of several parameters. This requires a type of data acquisition system called Simultaneous Sample and Hold (SS&H), used on the DT2809, DT2829, DT2838, and other models. SS&H systems use a separate sample and hold circuit on each input. When sampling begins, all circuits simultaneously switch to hold, freezing each input signal until it can be sampled by the A/D converter. By contrast, conventional data acquisition systems use a single sample and hold circuit, and must sample inputs sequentially.

Simultaneous sampling is also a characteristic of delta-sigma A/D converters, such as those used on the DT3818 Fulcrum Delta Sigma Series. Since delta-sigma designs use a separate A/D converter per channel, it is possible to sample all inputs simultaneously.

**Speed  
(Throughput, Aliasing,  
Acquisition Time,  
Conversion Time,  
Transfer Time, Overlap)**

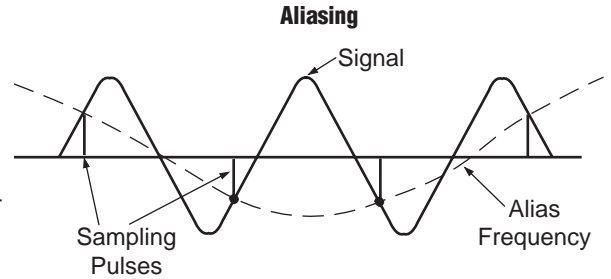
Speed is always a consideration in data acquisition.

In audio, radar, destructive testing, and other high-speed applications, the rate at which data can be sampled—also called throughput—is often the most important factor in choosing a data acquisition board. Data Translation specifies throughput in mega and kilosamples per second (MS/s and kS/s): a board with 250 kS/s A/D throughput can sample inputs 250,000 times per second, and transfer the resulting data to system memory.

In cases where multiple A/D converters are used on a single board, such as the DT3818 Fulcrum Delta Sigma Series, the specified board throughput represents the aggregate, or sum total, of the individual converter throughputs.

According to sampling theory (the Nyquist Theorem), a data acquisition system should sample an input signal at least twice as fast as the input's highest frequency component. That is, to measure a 20 kHz sine wave, the A/D throughput should be at least 40 kS/s.

This avoids an error condition called aliasing, in which very high frequency



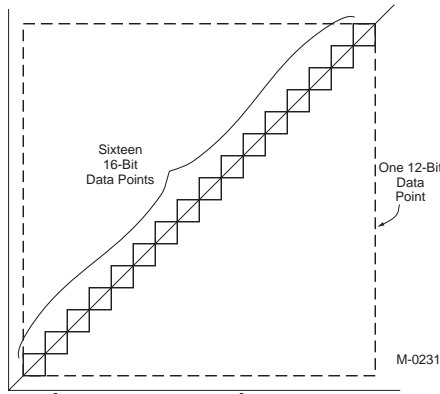
By sampling too slowly, aliasing occurs: The input signal is represented by a lower frequency value. This erroneous alias frequency cannot be distinguished from valid data.

input components appear in the digital code as erroneous lower frequencies. Where the input's frequency content is unknown, many users sample at the highest frequency they can, or remove very high frequencies by passing the input through a low-pass filter (such as the antialiasing filters built into some data acquisition boards). Boards using delta-sigma converters have very effective built-in anti-aliasing filters due to their high speed sampling and built-in DSP.

Since conventional analog input circuits share a common A/D converter, the number of input channels in use usually affects throughput. If you wish to sample four channels at 40 kS/s each, you need a data acquisition system with a throughput of at least 160 kS/s (4 inputs times 40 kS/s/input equals 160 kS/s). Delta-sigma A/Ds, such as those used in Fulcrum Delta Sigma, are an exception: In these each channel has its own A/D converter.

**Resolution, Ranges, and Bit Weights**

Resolution (bits)	Number of Counts	dB	% of Range	LSB Value			
				±10 V Range	±5 V ±0-10 V Range	±1.25 V, 0-2.5 V Range	±.02 V Range
8	256	48.2	.39%	78 mV	39 mV	9.8 mV	.16 mV
10	1,024	60.2	.098%	20 mV	9.8 mV	2.4 mV	.04 mV
12	4,096	72.2	.024%	4.9 mV	2.4 mV	.61 mV	.01 mV
16	65,536	96.3	.0015%	.31 mV	.15 mV	.04 mV	.0006 mV
20	1,048,576	120.4	.000095%	—	—	—	—
24	16,777,216	144.5	.000006%	—	—	—	—



A 16-bit converter provides 16 times as many points as a 12-bit converter operating over the same range:  $\frac{2^{16}}{2^{12}} = \frac{65,536}{4,096} = 16$

Three elements determine A/D throughput: conversion time, (the time needed to do the actual A/D conversion); acquisition time (the time needed by associated analog circuitry the multiplexer, amplifier, and sample and hold—to acquire a signal accurately) and transfer time (the time needed to transfer data from the board to system memory). (Issues affecting transfer time can be complex; these are discussed in a later section on data transfer.)

Normally, a board first acquires a signal and then converts it. Throughput is determined by the sum of the conversion time and the acquisition time. High speed Data Translation boards (such as the, DT3010, DT31-EZ, DT2831, and DT2821) increase throughput by overlapping the acquisition time on one sample with the A/D conver-

sion time of the previous sample. In effect, the A/D circuitry handles two signals at one time.

The high gains associated with .1 and .02 V input ranges necessarily reduce throughput. Like any amplifier, the onboard programmable gain amplifier's bandwidth (or speed) reduces as its gain increases. Because of this, many data acquisition boards uniformly extend the acquisition time for all gains and so reduce throughput from 50 kS/s, for example, to 2.5 kS/s.

### Accuracy (Resolution, LSBs, ENOB, THD)

Accuracy—how closely the binary code matches the incoming or outgoing analog signal—is also important. It can be a deciding factor when the analog signal contains much information (as an audio signal does), or when you must examine a small part of the range in great detail (as in chromatography applications). Data Translation products typically specify accuracy in terms of system error. The unit is percent of full-scale range. System error takes in all sources of error, including analog noise, system nonlinearities, and reference variation.

The major component of A/D or D/A accuracy, and its limiting factor, is resolution. Given in bits, resolution determines the number of counts or number of binary numbers used to represent the analog signal. Twelve-bit converters, for

example, can assume 212 different states and so divide their ranges into 4,096 pieces. This translates into digital code that track the analog signal to within .024% of the range. More bits yield exponentially higher resolution.

Another measure of resolution is the least significant bit or LSB—the smallest change in the analog signal that the digital code can represent. LSBs are specified both as a percent of range and as the smallest voltage change that can be resolved on a particular range.

While these dc accuracy measurements are crucial, it is the ac characteristics of an A/D circuit that determine how accurately it digitizes complex waveforms. Errors introduced by nonlinearities, aperture uncertainty, noise, quantization, and other sources of signal distortion are involved in determining the Effective Number Of Bits (ENOB) an A/D circuit is capable of resolving in the frequency domain. Maximizing a board's ENOB, or making sure its ac performance is as good as its dc performance, involves meticulous system-level design, which considers the move from a data acquisition board an intricate analog component. Data Translation calculates ENOB according to the following formula:

$$ENOB = \frac{(S/(N + D)) - 1.76}{6.02}$$

### Pacer Clock Characteristics

Target Frequency	400 kHz Oscillator (2.5µs)			5 MHz Oscillator (.2µs)		
	Best Fit	Next Higher	Next Lower	Best Fit	Next Higher	Next Lower
15 kHz	14.8 kHz	16 kHz	14.3 kHz	14.97 kHz	15.02 kHz	14.93 kHz
50 kHz	50 kHz	57 kHz	44 kHz	50.0 kHz	50.5 kHz	49.5 kHz
150 kHz	133 kHz	200 kHz	100 kHz	147 kHz	152 kHz	143 kHz
250 kHz	200 kHz	400 kHz	100 kHz	250 kHz	263 kHz	238 kHz

## Data Conversion Technologies

	Conventional	Delta Sigma
<b>A/D Subsystem</b>		
<b>Overview</b>	Excellent for measuring dc and very high speed signals; excellent dc characteristics; single-point acquisition and real-time response; high speed dynamic performance	Excellent for measuring ac signals; high-accuracy ac measurement with built-in anti-aliasing filter
<b>Configurations</b>	12 or 16 bits; 7.5 kHz to 1MHz, aggregate throughput	16 bits at 52 kHz per channel
<b>Architecture</b>	One A/D with multichannel multiplexer	One delta-sigma A/D per channel
<b>Simultaneous Sampling</b>	Requires special SS&H circuitry; available on some models	All models
<b>Anti-Aliasing Filters</b>	Available on some models; typically uses 4-pole analog filter; cutoff frequency = 5, 10, or 20 kHz; -24 dB at twice cutoff frequency rate)	All models; digital filter provides "Brick Wall" filtering (-80 dB at 1.2 times cutoff frequency) automatically tracks speed of A/D converter
<b>DA Subsystem</b>		
<b>Overview</b>	Typically two 12 or 16-bit DACs; excellent dc characteristics	Typically two 16-bit delta-sigma DACs; excellent ac characteristics
<b>Output Filters</b>	Not available on all models; when available, typically 2-pole analog; cutoff frequency = 20 kHz; -12 dB at twice cutoff frequency	All models; uses a combination of digital and analog filters to reduce glitches and other noise sources more than 80 dB

One of the most common effects of poor A/D circuit design is the introduction of harmonic distortion in the analog signal path. Total Harmonic Distortion (THD) is a ratio of the sum of the harmonics of the fundamental frequency of the input signal to the fundamental frequency itself.

A circuit with high THD likely has a design weakness that produces these distortion errors. To minimize THD, the circuit design at the analog input must be flawless, eliminating nonlinearities with respect to the ac characteristics of the input signal.

### A/D Converter Types (Successive Approximation, Flash, Integrating, V/F, Delta Sigma)

The heart of a data acquisition board is its A/D converter. No single converter type can meet the signal-acquisition needs of all applications equally well, and several different classes of converters exist. Each has its own particular advantages and disadvantages.

A typical A/D converter contains an analog multiplexer, that chooses one from up to 16 analog input signals; an amplifier that buffers the analog signal and may also apply gain to boost its voltage level; a sample and hold circuit that holds the input signal constant during the actual conversion; and an A/D converter that changes the analog signal into a digital code.

Successive-approximation converters feed various binary codes into a D/A converter and then use an analog comparator to compare the resulting analog output with the sampled signal. Using what is essentially a binary search methodology, the binary code eventually settles on a number that most closely represents the value of the analog input signal. Successive-approximation A/Ds are relatively accurate and fast, although they can exhibit some nonlinearities and missing codes.

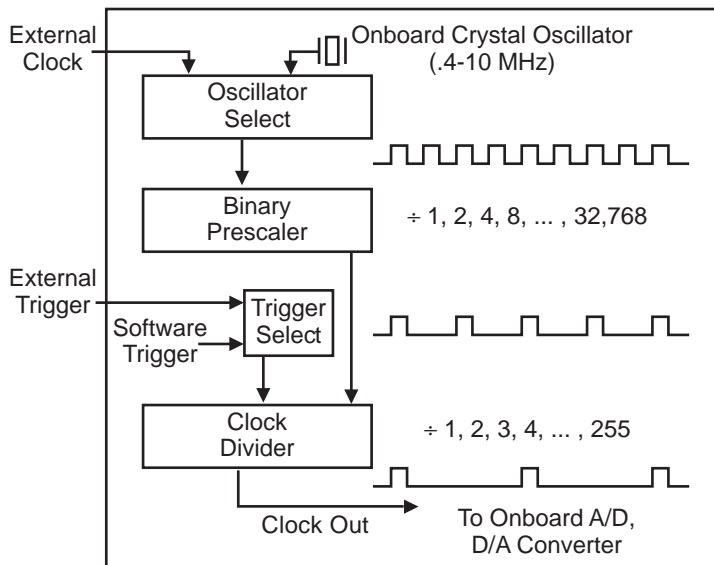
Parallel, or flash encoding is the fastest A/D conversion method. The input signal

is fed to  $2^{n-1}$  (where n equals the number of bits of resolution) analog comparators whose reference inputs are derived from equidistant taps off a linear resistor ladder. A priority encoder generates a digital output corresponding to the highest comparator activated by the input voltage. Unfortunately, flash encoders are prohibitively bulky and expensive for most applications, especially those requiring high resolution.

Several techniques including dual-slope use a capacitor to keep track of the ratio of an input signal to a voltage reference. These methods all average, or integrate, the input signal for a fixed time interval for each sampled measurement using a current source and a capacitor. Such integrating A/D converters have an important advantage: the output is proportional to the average input voltage over the integration time. By choosing a sampling interval that is a multiple of the power-line period, the converter becomes insensitive to 60 Hz "hum" (and its harmonics) on the input signal. The main disadvantage is that integrating A/Ds are relatively slow.

Voltage-to-frequency (V/F) methods convert an analog input voltage to an output pulse train whose frequency is proportional to the input level. V/F converters are relatively inexpensive and are useful when the converter output is to be used to digitally transmit a signal over a cable via carrier-signal modulation.

Delta-sigma A/Ds, such as those used in the DT3818 Fulcrum Delta Sigma Series, use fundamentally different conversion techniques optimized for tracking ac signals over time. Delta-sigma A/Ds typically use a 1-bit converter that greatly oversamples the input signal. Using circuitry built into the A/D converter, the resulting bit stream is accumulated and decimated to provide the desired resolution and word-sampling rate. Since they are mostly made up of digital components, delta-sigma



A typical pacer clock circuit can accept an onboard external frequency source, and a hardware or software trigger, and divides the frequency source by both a prescaler and a divider.

A/Ds exhibit exceptionally good ac performance, including noise, linearity, drift, monotonicity, accuracy, aliasing, and resolution characteristics.

Another benefit of delta-sigma A/Ds is built-in digital filtering that effectively eliminates aliasing. Very rapid “brick wall” attenuation of input frequencies

above the Nyquist frequency (half the sampling rate) is automatic.

The only disadvantage of delta-sigma converters is an inherent group delay. In Fulcrum Delta Sigma, for example, each data point is effectively an average of 18 conversion periods, an insignificant characteristic in most open-loop signal

processing and analysis applications, but possibly of concern in real-time control situations.

### Analog Outputs (Independent DACs, Settling Time, Deglitched Outputs, Reconstruction Filters)

Most Data Translation analog output circuits have a separate D/A converter (DAC) and data buffer for each channel. This permits outputs to be updated one-at-a-time or simultaneously (to change both channels of an XY plotter, for example). When two DACs are updated at a time the total throughput can be twice the single-channel throughput.

The major component in DAC throughput is settling time. While a DAC’s output begins to change as soon as it receives a new data value, the output is valid only after the analog circuitry has stabilized. Settling time is the period a DAC needs to reach rated accuracy after receiving an output change. Full-scale settling time is actually a worst-case value. Smaller than full-scale changes settle in less time. Settling time varies inversely with the size of the output change. Settling time is specified in microseconds ( $\mu$ s).

## Data Transfer Methods for IBM PC Data Acquisition Boards

Transfer Method	Bus	Maximum Throughput/Board	Continuous	Typical Models
PIO with Software Polling	ISA	20 kS/s	—	DT2815, DT2817
PIO with Interrupt	ISA	40 kS/s	—	DT2811, DT2814
Single-Channel DMA	ISA	100 kS/s	—	DT01-EZ, DT16-EZ, DT2801 Series, DT2812
Single-Channel DMA w/DT-Open Layers Driver	ISA	330 kS/s	✓	DT21-EZ Series, DT31-EZ, DT34-EZ
Dual-Channel DMA	ISA*	950 kS/s*	✓*	DT21-EZ Series, DT2821, DT2831, DT2839
REP INSW	ISA	330 kS/s	✓	DT31-EZ, DT34-EZ
DT-Connect	ISA	1MHz	✓	DT2839
To Onboard Memory	ISA	1 MHz	✓	Fulcrum, Fulcrum Delta Sigma
PIO with Interrupt	PCI	>330 kS/s	✓	DT300 Series
PIO with Interrupt	PC Card	100 kS/s	✓	PC Card-EZ
Bus Master DMA	PCI	1.25 MS/s	✓	DT3010, DT300 Series

\*Highest performance burst to memory achieved with DT2839 plugged into EISA Bus slot on high speed PC compatible. Continuous transfers occur at lower speed.

To provide a cleaner analog output signal, some Data Translation boards (DT2821 Series, for example) use a deglitching circuit. DACs produce glitches: rapid, high energy pulses caused by minute timing differences (skew) in the converter's data switches. The deglitching circuit holds the output constant for a brief period, then reconnects the DAC output after the glitch has passed.

Another way of reducing unwanted noise from an analog output is to pass the output through a low-pass reconstruction filter; this is a feature of Fulcrum DT3801 Series boards. The delta-sigma type DACs used in the DT3818 Fulcrum Delta Sigma Series construct an analog output signal by using an 8x interpolation filter followed by a 64x oversampling converter. This method automatically interpolates between data points to smooth the resulting analog output, giving the effect of much higher resolution. It also provides very steep "brick wall" filtering of unwanted output noise.

### Clocks, Triggers, and Counter/ Timers

**(Oscillator, Divider, Prescaler, Trigger)**  
To perform multiple conversions automatically at precisely-defined time intervals, many data acquisition boards are equipped with one or more pacer clock circuits. Where present, the pacer clock typically starts all conversions. Boards that permit simultaneous A/D and D/A operation (for example, DT3010, DT31-EZ, DT2831, and Fulcrum Series) often have separate A/D and D/A pacer clocks that can run at different rates.

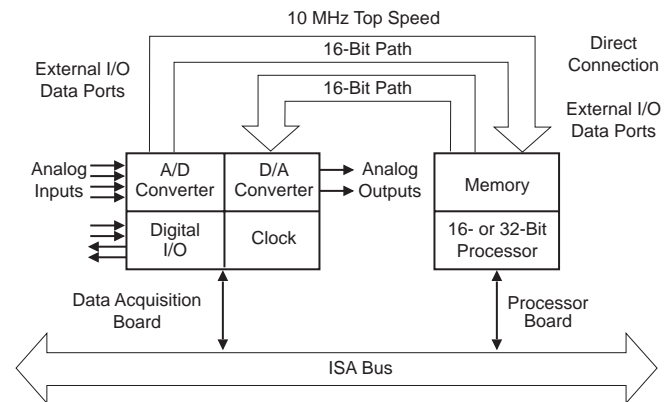
Pacer clocks are made up of a frequency source (either an onboard free-running oscillator between 400 kHz and 10 MHz, or a user-supplied signal) and a divider network that steps the frequency source down to more usable values—from less than 1 Hz to the maximum throughput of the board. The frequency source is also

called the clock's base frequency, and determines the granularity or distance between available settings. Higher base frequencies offer finer granularity, especially at high sampling frequencies. For example, values for a 400 kHz oscillator are 2.5  $\mu$ s apart; those for a 5 MHz oscillator are .2  $\mu$ s apart. Dividers can typically be set for any value within an 8- or 16-bit range. Some designs also use a binary prescaler before the divider to extend the clock's range.

Pacer clocks are started by triggers: either by a program instruction (a software trigger), or on receipt of a digital pulse or analog voltage at the board's connector (an external trigger). External clock frequency sources and external triggers help you synchronize data conversions with off-board events. An external trigger can serve as a gate to enable conversion, while with each tick, the external frequency source starts a new conversion. External frequency sources can also be used to produce clock frequencies that cannot be achieved with the onboard oscillator.

Converters on delta-sigma A/D and D/A converters, such as those used on Data Translation's DT3818 Fulcrum Delta Sigma Series, have an inherent "group delay" that introduces a latency period between the time a sampling window opens and the time valid data is actually available.

Delta-sigma A/D converters do not deliver the first valid data sample until 18 sample clocks after the start-to-acquire signal is given (the A/D group delay is  $1/f_s \times 18 \mu$ s). This delay is analogous to the group phase delay introduced by analog front end



*By providing dedicated high speed data paths, DT-Connect significantly improves data throughput.*

antialiasing circuits. Delta-sigma DACs have a 33-clock group delay.

Many data acquisition boards (for example the DT31-EZ, Fulcrum, DT300 Series, DT2831 Series, DT3010, and DT2819) also contain general purpose counter/timer circuits. These typically consist of several counters (digital circuits that count pulses) and a frequency source that, when used with a counter, forms a precision timer. Counter/timers can be used in dozens of configurations. Counters can be used singly or in combination with other counters, external or internal frequency sources, and gates. While extremely flexible, counter/timers can be difficult to use without software that easily configures the circuitry for commonly-used functions.

### IBM PC Data Transfer Methods (ISA Single DMA, ISA Dual DMA, ISA REP INSW, PCI Bus Master DMA, PCI Bus PIO, PC Card Bus PIO, DT-Connect™, Onboard Memory, FIFOs)

For high speed data acquisition, the method of data transfer is just as important as the speed of the A/D or D/A converter. Data Translation manufactures many series of IBM PC compatible boards for different I/O buses, and differing methods of data transfer (the means by which data values are transferred between the board and computer memory).



## ISA Bus IBM Compatibles

The DMA (Direct Memory Access) method matches the speed at which data is transferred to converter speeds. As the name suggests, DMA data transfers establish a direct link between a data acquisition board and the host system memory. Once they are set up, DMA transfers occur without intervention from the host CPU. On PC clones, single-channel DMA boards, equipped to access a single DMA channel only, can easily handle the DT01-EZ's or DT2801 Series' maximum throughput of 27.5 kS/s; higher performance clones can achieve throughputs to about 100 kS/s. However, due to the design of the ISA Bus, only 64 ksamples can be transferred at once using a single DMA channel. Then, the DMA controller on the host must be reprogrammed.

The next performance threshold for ISA Bus boards, up to 250 kS/s to and from memory, requires dual-channel DMA data acquisition boards (such as the DT21-EZ Series, DT31-EZ, DT2821, DT2831 Series) on IBM PC compatibles. Because they are PC AT-compatible, these boards perform 16-bit data transfers. This immediately doubles their throughput. Because two DMA channels are used, the overhead associated with reprogramming one DMA channel (necessary when the defined DMA buffer fills) can be overlapped with data transfers using the other DMA channel. This permits the board to perform data transfers without interruption.

Dual-channel DMA equips a host computer with the fastest processor speed you can find. At this point, maximum DMA throughput is pretty much limited by the speed at which data can be transferred out of main system memory and onto hard disk for storage. To ease this transfer bottleneck, choose a hard disk optimized for high speed (access time 220 ms) with a high speed controller (ESDI or SCSI). In addition, software for dual-DMA boards

often supports the PC's full 16 Mbyte extended memory space or the 32 Mbyte LIM (Lotus®-Intel®-Microsoft) defined expanded memory space.

A proprietary software technique used in Data Translation's DT-Open Layers drivers lets you achieve high-speed continuous data transfer on the ISA Bus using a single DMA channel. This is achieved by creating a circular software buffer so that data can be continuously loaded into one location in the buffer while values are read out of another location. When the end of the buffer is reached, the driver automatically reprograms the computer's DMA controller, and values are redirected to the beginning location in the buffer. This process can continue indefinitely.

PCs using 386, 486, and Pentium-compatible processors feature a special data movement instruction called Repeat Instring Word or REP INSW. This highly efficient programmed I/O instruction allows the processor to use a very small amount of overhead to move blocks of data to and from sequential locations in host memory. Because it doesn't have to keep track of actual address locations, REP INSW can quickly move words into or out of a data acquisition board, simply incrementing a memory-location pointer after each move. Because the block-move parameters are all set up in advance, REP INSW is very much like a classic DMA process, except here, the processor acts as the DMA controller.

## PCI Bus High Performance Data Transfers

Along with the cost-maturation of Pentium-class PCs comes a rise in the use of the PCI (Peripheral Component Interconnect) the bus for high-speed data acquisition. PCI's 132 Mbyte/s, 32-bit data pathways are more than an order of magnitude faster than the ISA Bus, making the bus ideal for high-performance data acqui-

sition boards such as Data Translation's PCI-EZ.

In fact, the PCI Bus is fast enough so that all subsystems on the board—A/D, D/A, and digital I/O—can operate simultaneously, at full throughput, without interruption, up to the limits of available system memory! Not only does the PCI Bus simplify hardware installation through its Plug 'N Play facilities, its direct accesses to memory through the system's PCI controller allows a data acquisition board to directly access system memory at the full speed of the PCI Bus, using fast programmed I/O operations, without incurring the cost of special DMA hardware. For more information on the benefits of the PCI bus for your data acquisition application, see page 148.

## PC Card Bus Programmed I/O

The Personal Computer Memory Card International Association (PCMCIA) has defined a standard for extremely compact (credit card sized) external plug-in circuit boards that add capabilities to host computers. These PC Card Bus boards are designed primarily for use with portable computers. They replace conventional backplane-mounted circuit boards with smaller, more power-efficient devices. Data Translation's PC Card-EZ Series data acquisition boards provide high-performance analog and digital I/O in any PC compatible that can run Microsoft Windows and has an available PC Card Type II or Type III slot.

While PCMCIA devices are designed to be Plug 'N Play under Windows, many PCMCIA require that you replace a piece of system software, Card and Socket Services, with a custom version that supports only the device being added. Thus, swapping PCMCIA devices requires changing software. All PC Card-EZ models support true Plug 'N Play operation

using our exclusive card management software. This software that ships with all PC Card-EZ products lets you run the PC Card-EZ in virtually any PCMCIA slot.

### Onboard Memory

Another very high-speed method of data transfer is possible when the data acquisition board has extensive onboard memory. This transfer to onboard memory can occur at any rate you desire, limited only by the speed of memory and control logic on the board. Data Translation's Fulcrum™ DSP data acquisition boards, for example, support transfer rates of over 4 MHz—far faster than the A/D converters themselves can run!

To speed data transfer to the host bus, many boards provide built-in FIFO data buffers. This onboard memory permits the board to transfer large amounts of data to or from the host at one time, overcoming bus contention and latency problems. FIFO data buffers are a feature of the PC Card-EZ™, DT3010, DT300 Series, DT31-EZ, DT2831, and DT2839 boards.

### Data Integrity (Continuous Performance)

If you are scanning channels in a particular sequence, missing one data point can cause all subsequent values to be misinterpreted. Short-lived, very high-speed phenomena may show up in only a few samples; missing one point can cause you to mistake an important event for noise or statistical error.

To assure data integrity, Data Translation has developed boards and software, including our powerful HP VEE and DT VPI visual programming environment, that support continuous performance, gap-free data transfers to and from memory or hard disk. Data Translation holds a patent on continuous performance techniques used on the Q-bus. Many additional methods have been developed over several years to accommodate different computer buses, board architectures, and throughput requirements. Continuous performance data acquisition is provided by the combination of HP VEE with the

DT VPI, DTx-EZ, or DataAcq SDK; and a DT21-EZ Series, DT31-EZ Series, DT3000 Series, PC Card-EZ, DT2821 Series, DT2831 Series, DT3010, or DT300 Series data acquisition board.

All continuous performance products share the ability to transfer data streams of arbitrary length to and from memory or hard disk at high speed—up to the maximum throughput of the board. Data acquisition using these products is typically limited in duration only by the amount of available memory or hard disk space. To assure that you have not missed a data value, most continuous performance boards contain error flagging circuitry that sets any time a new data value overwrites a previous value.

### Software

**(HP VEE and DT VPI for Windows, DT-Open Layers, DTx-EZ, DataAcq SDK, Drivers, and DSP LAB)**

Data Translation boards are supported by a variety of software products, aimed at a wide range of users. This includes HP VEE

## Board Features Supported by DT-Open Layers Software

	Continuous Transfer			Max Throughput	Simultaneous A/D & D/A	
	1-Channel DMA	2-Channel DMA	Other		High Speed Continuous	Single Conversion
DT2801 Series	✓	—	—	Board-Limited	—	✓
DT2812, DT2812-A	✓	—	—	Board-Limited	—	✓
DT2821 Series	—	✓	—	Board-Limited	—	✓
DT2831 Series	D/A only	✓	—	Board-Limited	—	✓
DT2839	✓	✓	—	>950 kS/s	✓	—
DT01-EZ, DT16-EZ	✓	—	—	Board-Limited	—	✓
DT21-EZ, DT23-EZ, DT24-EZ, DT24-EZ-PGL	✓	✓	—	Board-Limited	—	✓
DT31-EZ, DT34-EZ	✓	✓	—	Board-Limited	✓	—
DT2811-PGH, DT2811-PGL, DT2814, DT2815, DT2817, DT2819	—	—	—	<500 kS/s	—	DT2811 only
DT300 Series	—	—	✓	Board-Limited	—	✓
DT3001, DT3002, DT3003, DT3004, DT3005	—	—	✓	Board-Limited	✓	—
DT7101, DT7102	—	—	✓	Board-Limited	—	✓

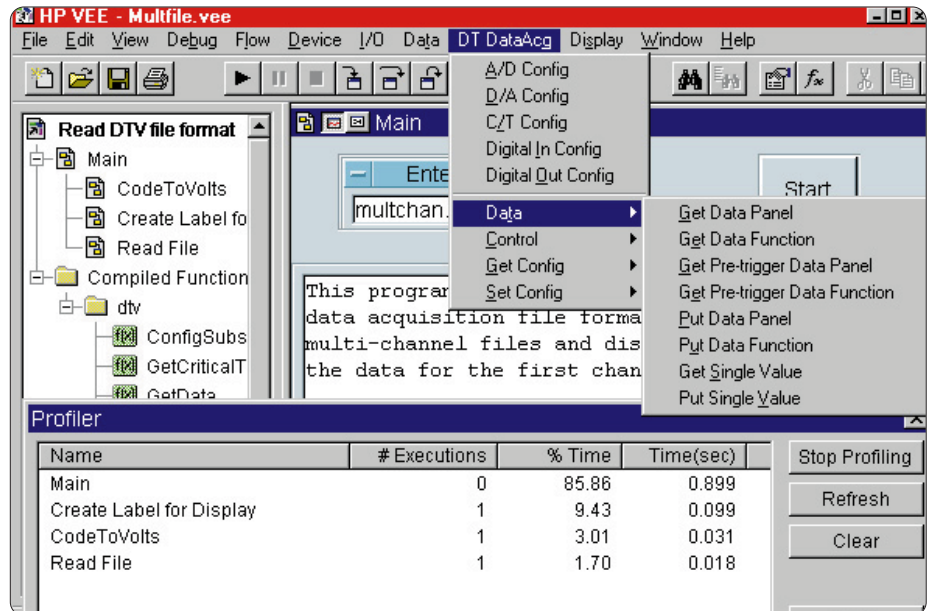
and DTx-EZ for Windows that performs data acquisition, analysis, and display at the click of a mouse button and the DataAcq SDK and DTx-EZ for programmers wishing to create custom applications. Many popular third-party application software products also support Data Translation boards. Contact the Data Translation sales department for details.

Our modular DT-Open Layers architecture isolates application software from hardware specific commands, automatically ensuring complete portability of DT-Open Layers compliant application code, including HP VEE, between compatible data acquisition boards. This application-level hardware independence allows hardware upgrades without reprogramming—your software development investment is protected. Nearly all Data Translation data acquisition boards are shipped complete with a DT-Open Layers software driver.

Data Translation's premier data acquisition visual programming language is HP VEE with DT VPI for Windows. With native versions for Windows 3.1, and Windows 95 and Windows NT, HP VEE lets you build better tests faster using an intuitive graphical user interface.

Our DTx-EZ ActiveX™ Controls for Visual Basic and Visual C++ for Windows programming tools is a set of ActiveX controls for data acquisition and display. DTx-EZ is also compliant with DT-Open Layers and provides controls that greatly simplify setup of the data acquisition board and they acquire and display data values.

DataAcq SDK™, a Windows function library offers C and C++ programmers maximum flexibility for development of DT Open Layers compliant application code for Windows 3.1/95 and Windows NT.



HP VEE with DT VPI

A powerful programmer's package is available for Fulcrum and Fulcrum Delta Sigma DSP data acquisition boards. DSP LAB provides efficient data acquisition, DSP math, logical operations and filtering using Fulcrum and Fulcrum Delta Sigma's built-in C40 processor. DSP LAB provides lower-level operation and full power for programmers. It provides a C programming environment for operations with the host, and the industry-standard SPOX™ DSP development environment for C40 programming.

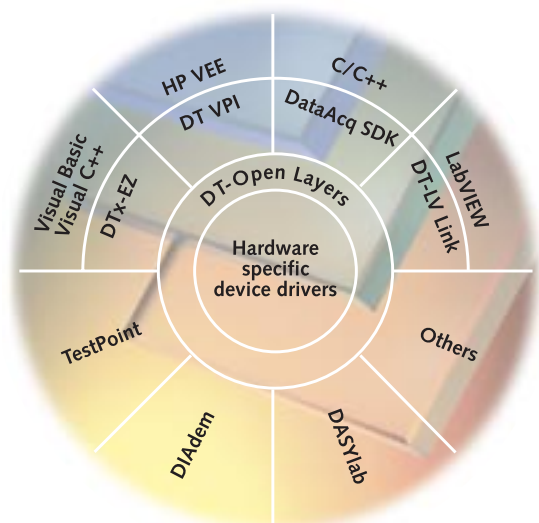
### High Performance Data Acquisition (Simultaneous A/D and D/A, Real-Time DSP)

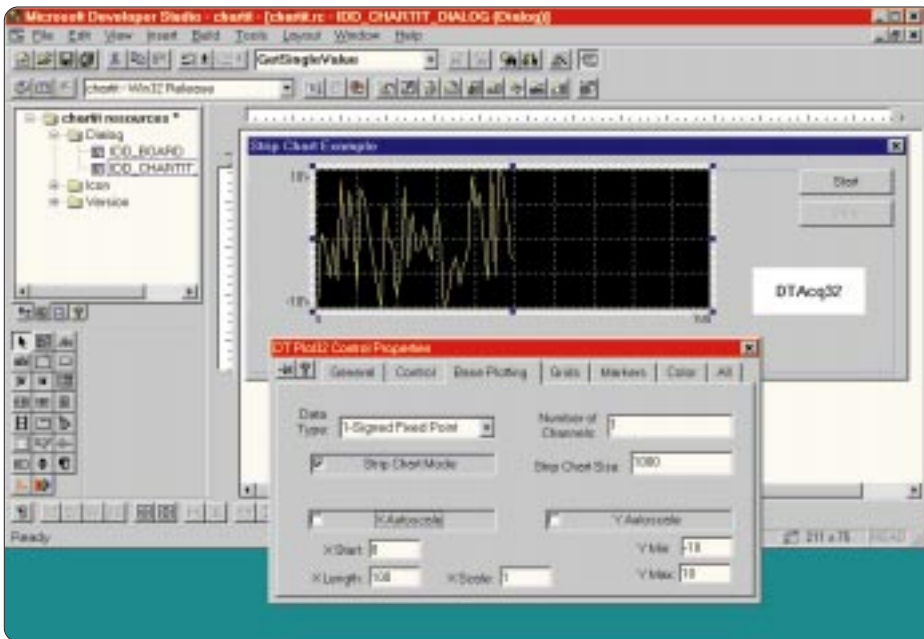
At the outer reaches of data acquisition stand a few advanced techniques developed by Data Translation to overcome specific computer limitations.

Simultaneous A/D and D/A transfers are possible on some high-speed multifunction boards, a feature very convenient for process control,

audio recording and playback, and so on. The methods used vary from board to board, and may involve use of multiple DMA channels, an onboard chip that timeshares a single data bus, or onboard input and output data buses each connected to a separate DT-Connect or onboard processor port.

High-speed data transfer can present some daunting data storage and processing problems: at 1 MHz, every second you accumulate one million 16-bit data words!





ActiveX controls for Visual basic and Visual C++

High-speed, DT-Connect-linked processors and real-time, application-specific DSP processors built into data acquisition boards can provide the solution.

For real-time applications that require absolutely deterministic, simultaneous data collection and analysis, Data Translation's Fulcrum family tightly couples high-performance A/D and D/A front-end circuits with the industry's leading floating-point digital signal processor. The result is a deterministic acquisition/analysis system that operates independent of the host computer, freeing up the PC for display and supervisory tasks.

### For More Information

For additional information on Data Translation products, contact your local distributor, the Data Translation home page (<http://www.DataTranslation.com>), or the Data Translation Sales Department.

### Compatible Products

Consult your Data Translation sales representative for a complete listing of hundreds of hardware and software products compatible with Data

Translation data acquisition and image processing products.

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