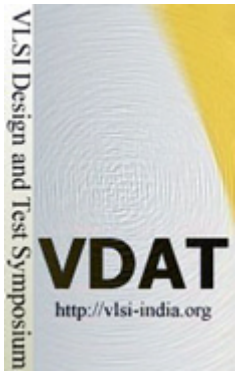

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15th VLSI Design and Test Symposium

To promote applications and research related to all aspects of VLSI in India

July 7-9, 2011

Wipro Technologies, Hinjewadi, Pune, India

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July 7, 2011 (Thursday)			
08.30 AM - 9.30 AM	Registration and Breakfast		
09.30 AM - 11.00 AM	**1A-1: Tutorial - T1-A** **Analog & RF Design** **Room A** **Fundamentals & Design of Phase-Locked Loops (PLLs)** Dipankar Nagchoudhuri, Subhajit Sen, and Chetan Parikh (DAIICT, Gandhinagar) 56 (Half-day Tutorial)	**1B-1: Tutorial – T2-A** **Automotive SoC** **Room B** **Challenges in the Physical Implementation of Automotive SoC's in RFCMOS65** Madhu Kiran, and Christian Joseph (NXP Semiconductors) 43 (Half-day Tutorial)	**1C-1: Tutorial – T3-A** **VLSI Design & Test** **Room C** **An Overview of Modern-day VLSI Design & Test Practices** C.P. Ravikumar (Texas Instruments India)
11.00 AM - 11.30 AM	Tea Break		
11.30 AM - 01.00 PM	T1-A Continues	T2-A Continues	T3-A Continues
01.00 PM - 02.00 PM	Lunch		
02.00 PM - 03.00 PM	**1A-2: Tutorial – T1-B** **Future directions in IC technology for RF communication: Challenges and Opportunities** Rajnish Sharma (CIET, Chandigarh) 32 (Half-day Tutorial)	**1B-2: Tutorial – T2-B** **Challenges in Automotive Chip Testing for Power Consumption & Analog-Mixed Signal Tests** Janardhan E, Venkatesh S S, and Saurabh Patodia (NXP Semiconductors India Pvt. Ltd) **60** (Half-day Tutorial)	T3-A Continues
03.00 PM - 03.30 PM	Tea Break		
03.30 PM - 05.30 PM	T1-B Continues	T2-B Continues	T3-A Continues
End of Day-1			

The speakers are expert practicing professionals in the respective areas. More details of the tutorial and biographies of the speakers are available from the VDAT website - http://vlsi-india.org/events/vdat2011/

Information

Please watch updates on VDAT at http://vlsi-india.org/ The idea behind the VLSI Design And Test (VDAT) Symposium is ***to promote Research and Development on all aspects of VLSI in India****. This symposium is a forum for free discussion of hot and emerging topics in VLSI. It provides a meeting place for VLSI professionals working in India and abroad. We have been holding this event since 1998, and the participation in the event has steadily gone up every year. The VLSI Industry in India and academic community working in the area of VLSI has provided immense support to the symposium.*

VDAT is sponsored by the ***VLSI Society of India****. Please consult http://vlsi-india.org/vsi/ for more information on goals, activities of the VLSI Society of India. To become a member of the VLSI Society of India, you can download the form from http://vlsi-india.org/vsi/membership/index.shtml (form is also included at the end of this document).*

Venue Information:

The symposium will be conducted at the Learning Cent re located in the campus of Wipro Technologies, Pune. Please refer the map for directions to Wipro campus.

The Pune Development Centre of Wipro Technologies is located in phase I of Rajiv Gandhi Infotech Park, Hinjewadi, Pune, and is 25 kms from the heart of Pune city. Pune city, a major railway junction, is easi ly accessible by air, train, and bus. Pune and Mumbai are well connected by the express highway.

Wipro Technologies
Plot No 2, MIDC – Phase I
Rajiv Gandhi Infotech Park, Hinjewadi
Pune – 411 057. India
Distances:
Pune Airport: 35 kms
Pune City: 25 kms

Speakers will have facilities such as DLP projector, cordless microphone, and whiteboard.

For a larger image of the route map:
http://vlsi-india.org/events/vdat2011/wipro-map-pune.jpg

Track T1 - Analog & RF Design
Tutorial – T1-A

Fundamentals & Design of Phase-Locked Loops (PLLs) (Half-day Tutorial)
Dipankar Nagchoudhuri, **Subhajit Sen**, and **Chetan Parikh** (DAIICT, Gandhinagar)

Abstract: Phase locked loops (PLLs) have become an integral part of many communication systems, as well as many digital and control systems, and have found applications in diverese areas such as, frequency and phase demodulation, doppler radar, satellite communication, frequency synthesis, clock generation and recovery, automotive electronics, servo control, reduction of jitter in highfrequency circuits, grid connected power systems, etc.
Conceptually as well as pedagogically, PLLs remain a tough subject. And in spite of their widespread use, they do not find more than a very basic treatment even in graduate-level courses in analog circuit design. Immense research and development has occurred in the types of PLLs available today. This tutorial proposes to offer an introduction to PLLs, starting from the basics – conceptual, mathematical, and circuit-level – and provide an overview of the design of PLLs, as well as of the research literature on PLLs.

Dr. Dipankar Nagchoudhuri is a Professor at DA-IICT. Previously, he was at IIT Delhi for about thirty years, and a Professor there from 1982. During this period, he held the position of Philips Chair Professor for about two years. He has also been a visiting faculty to University of Malaya, Kuala Lumpur, a Visiting Professor at Siemens AG, Munich, and at Instituto Nacional de Astrofisica, Optica y Electronica, Mexico. He has authored three books: Semiconductor Devices (1989), Microelectronics Technology (1998) and Microelectronic Devices (2001). He has published numerous papers in National and International Conferences. He has guided about a dozen PhD theses and taught undergraduate and graduate courses in electronics. He was awarded the best teacher award in 1980-1981 by the EE Students Society. His research interests are in CMOS technology and circuits.

Dr. Chetan Parikh obtained his B.Tech. from the Indian Institute of Technology (IIT), Bombay, in 1985, and his M.S. and Ph.D. degrees from the University of Florida, Gainesville, in 1988 and 1992, respectively, all in electrical engineering. In 1992-93, he was a post-doctoral fellow at the University of Florida. From 1994 to 2000, he was on the faculty of IIT-Bombay, as an Assistant (1994-98) and Associate Professor (1998-2000). He was then a Visiting Associate Professor at the University of Missouri - Rolla (2000 - 2001), and at Purdue University (2001 - 2002). Then he worked at Motorola in Austin, Texas (2003 - 2004). From July 2004, he has been at the Dhirubhai Ambani Institute of Information and Communication Technology (DA-IICT), Gandhinagar, where currently he is a Professor. He has had sponsored and consultancy projects from government agencies (DST, DOE), as well as industries (TI, National Semiconductors, GE). His current research interests are in analog and mixed-signal CMOS circuit design. He has published more than 30 papers in journals and conferences, and has presented tutorials on analog circuit design at VDAT-2005, VDAT-2007, ST Microelectronics, and at other national level workshops.

Dr. Subhajit Sen obtained his B.Tech Degree from Institute of Technology, BHU, his M.S from Louisiana State University, and his Ph.D. (in analog VLSI design) from University of Waterloo, Canada, in 1997. He has worked at Cypress Semiconductor as Project Manager from December 1997 to February 2000, Project Manager at Cirrus Logic from July 2001 to October 2007, Senior Principal Engineer SiRF Technology from November 2007 to January 2009. From February 2009, he has been an Associate Professor at Dhirubhai Ambani Inst. of Information & Communication Technolgy. His research interests are analog circuit design using CMOS & bipolar technologies, analog interface circuits for CMOS SOC's, phaselocked loops, temperature-sensors, low-power CMOS circuits, biomedical instrumentation, and non-linear analysis of electronic circuits. He is currently working on CMOS line-driver circuit design, auto-tuning circuit design and audiometer design (for measurement of hearing impairment) using FPGA technology.

Tutorial – T1-B

Future directions in IC technology for RF communication: Challenges and Opportunities (Half-day Tutorial)
Rajnish Sharma (CIET, Chandigarh)

Abstract: Since the predictions made by Moore about the reduction of feature size of electronic devices, there has been a consistent growth in integrated circuit technology in terms of not only pushing the size of the devices to almost around 0.13 micron, but also putting them into new applications everyday. RF communication market has really expanded exponentially since the first mobile phones hit Indian market sometime toward the beginning of this century.
Accordingly, it remains a challenge to design electronic devices suiting the requirements of the RF communication to meet the daily upcoming challenges like higher integration levels, lower power dissipation, smaller form factor and lower cost in portable battery powered RF transceivers for personal communication applications.
India had over 14.17 million mobile phone subscribers by May 2003, about 102.8 per cent more than the previous year and this number is expected to rise to over 160 million by 2012. Design of an integrated circuit at Radio Frequencies is unique in the sense that it draws upon many disciplines unrelated to integrated circuits directly. At such a high value of frequencies, normal electronic components likewise resistors, capacitors, inductors and Bipolar Junction Transistors (BJTs) etc. refuse to work as per their normal behavior. Many more additional effects start playing their roles, which ought to be taken into account by an RF IC designer.
In this tutorial, the presenter proposes to cover some very basic fundamentals of electronic devices for design of Integrated Circuits meeting the challenges pertaining to requirements of RF communication. Tutorial will also cover the detailed design of a typical RF Low Noise Amplifier (LNA), which remains one of the most important circuit block of an RF Transceiver architecture.

Rajnish Sharma is a postgraduate and doctorate in Electronic Science from Kurukshetra University, India. He completed all his experimental work for his Ph.D. as a part of Government of India sanctioned project at National Physical Laboratory, New Delhi. He has got about six years of teaching experience at BITS, Pilani, where he taught a course on RF Microelectronics quite a number of times to ME (Microelectronics) students. Currently, he has been working with Chitkara University as Dean Academics in School of Engineering and technology and takes care of all the administrative responsibilities toward setting up one of the most challenging and fruitful academic system for engineering students. Passionate about teaching, he is an active researcher too.
Currently, he is pursuing his research interests in area of RF circuit design and also working for a project sanctioned by Government of India. He has got one book by Oxford Publications and about 15 research papers to his credit. He has presented his research work at various national and International platforms like MRS Symposium (USA), RNL (Denmark) and ASEE (Hungary).

Track T2 - Automotive SoC

Tutorial – T2-A

Challenges in Automotive Chip Testing for Power Consumption & Analog-Mixed Signal Tests (Half-day Tutorial)
Janardhan E, **Venkatesh S S**, and **Saurabh Patodia** (NXP Semiconductors India Pvt. Ltd)

Abstract: With the advent of growing complexity in the design of automotive chips, the process of IC testing is getting far more complex and expensive. Traditionally, low speed scan was measured against the test coverage metric and would suffice most test requirements, but now the emphasis being on quality more than ever, at speed testing becomes a necessity in the testing arena. To improve test-timings, the scan shift frequency is increased, which in-turn leads to higher power consumption during testing than the functional mode of the chip. This can give rise to serious problems like instant circuit damage; increase product costs, decreased system reliability and decrease of overall yield.
As we move towards systems on silicon, highly integrated interfaces to the analog world become common place. Typical circuits contain a mix of digital, mixed-signal and analog cores. The mixed-signal modules are either digital in/analog out or analog in/digital out. In all cases, digital control inputs are assumed to be present along with the signal path. The development of such devices requires fast time-to-market cycles and reuse of building blocks.
This tutorial discusses various ways to generate “power-efficient” patterns with low switching activity and ensuring the impact on pattern volume and test coverage metrics are mitigated, thereby deploying a good test solution. The tutorial also discusses about defining a standard test access methodology for embedded analog/mixed signal blocks to enable reuse of test access methodology, hardware and test programs as far as possible, to keep the test time as low as possible.

Janardhan Eerappa is working as a Senior Architect in Business Unit Automotive Solutions in NXP Semiconductors India Pvt Ltd. He has been with NXP for 6 months. In his role, he is involved in defining DfT Architecture, DfT Implementation and validation of SoC’s for NXP Automotive products. Prior to this he was involved in the DfT activities for various wireless, telecom, multimedia and network ASIC and SoCs for different clients. He has B.E in Electronics and Communications from BMS College of Engineering, Bangalore. He has total 12 years of industrial experience in VLSI.

Venkatesh S S is working as a Architect in Business Unit Automotive / Business Line Car Entertainment Solutions in NXP Semiconductors India Pvt Ltd. He has been with NXP / Philips for 10 years. In his role, he is involved in the development of SoC’s for NXP Automotive products. Prior to this role, he was involved in DFT and STA activities, which include flow development and design activities for NXP Design Community. He has B.E in Electronics and Communications from Rural Engineering College, BHALKI, Karnataka. He has total 10 years of industrial experience in VLSI.

Saurabh Patodia is working as Senior Design Engineer with NXP Semiconductors India Pvt Ltd. for the past 3 years. In his present role, he is working on the deployment of DFT techniques in Automobile ASICs. In his previous role, he was involved in System Design and Virtual Prototyping for products in various business units inside NXP Semiconductors. He has B.E in Electronics and Communications from R.V. College of Engineering, Bangalore. His interests encompass VLSI System Design and Testing.

Tutorial – T2-B

Challenges in the Physical Implementation of Automotive SoC’s in RFCMOS65 (Half-day Tutorial)
Madhu Kiran, and **Christian Joseph** (NXP Semiconductors)

Abstract: The RFCMOS based SoC’s are the order of the day for automotive applications. The integration of RF blocks in SoC’s coupled with stringent automotive quality requirements make the physical design aspects much more complex. With the technology shrinking to deep sub microns, the integration of RF blocks together with high frequency digital logic in SoC’s is very challenging. In RFCMOS SoC’s, not only the capacitive coupling but also the magnetic coupling comes into effect, making the integration much more difficult. If proper design care is not taken, the clock spurs impact the RF spectrum, leading to partial or complete functional failure.
This tutorial discusses the various components which deteriorate the baseband spectrum such as magnetic & electrical coupling, coupling through ground / supply rails, substrate coupling and thermal coupling. This also address the physical design community about how to tackle the noise being propagated to RF baseband broadly at two different levels of RFCMOS SoC integration one being the interference generated on-chip stage and another the interference being injected from off-chip. In on-chip stage, the different techniques of clock selection, architecture selection, floor-plan considerations and substrate noise isolation techniques and effective implementation would be discussed. In off-chip stage, selection of right packages, splitting of different power and grounds in the design would be described.

Madhu Kiran is working as the Senior Technical Leader in Business Unit Automotive / Business Line Car Entertainment Solutions in NXP Semiconductors India Pvt Ltd. He has been with NXP / Philips for 5.5 years. In his role, he is involved in the development of SoC’s for NXP Automotive products. Prior to this role, he involved in the physical design activities for cell phone processors SoC’s, UWB Soc’s and Set Top Box SoC’s for various business units inside NXP. He has B.Tech in Electronics and Communications from Nagarjuna University, A.P. and M.E. in VLSI Design from PSG Tech, Bharatiar Univiery, Taminadu. He has 9 years of total industrial experience during which he also worked for Cadence Design Systems and Bharat Electronics Limited. His interests span to VLSI Design and ASIC developments.

Christian Joseph is working as Principal Design Engineer in Business Unit Automotive / Business Line Car Entertainment Solutions in NXP Semiconductors Hamburg (Germany). He has been with NXP / Philips for 23 years. In his role he was working as Integration Team Lead for a 65nm RFCMOS NXP Automotive product. Prior to this role, he was involved in product development, design for test and physical design for various business units inside NXP. He has M.E. in Electronics and Computer Engineering from university of applied sciences, Luebeck/Germany.

Track T3 – VLSI Design & Test
Tutorial – T3-A

An Overview of Modern-day VLSI Design & Test Practices (Full-day Tutorial)
C.P. Ravikumar (Texas Instruments India)

Abstract: The goal of this tutorial is to help faculty from engineering colleges, who are involved in teaching VLSI oriented courses, to get to know some of the important cutting edge practices in the areas of VLSI design and test. Today, VLSI design has been included as a core subject in most undergraduate programs in Electronics Engineering in India. Over 50 M.Tech programs in VLSI Design have been introduced. However, there are several problems in teaching the courses related to VLSI

a. In many colleges, the faculties who are teaching the courses are not aware of current practices. As a result, there is a large gap in what is being taught and what is being practiced. This impacts the semiconductor industries, since the graduating engineers have to be retrained.
b. The VLSI field is constantly changing, making the industry-academia gap wider each passing year. Yet, many faculty depend on text books that were written many years ago.

Tutorial contents:

- Design Flow – We will introduce the modern-day SoC design flow and discuss the issues involved in IP design and integration. (1 hr)
- Multicore SoC – We will examine the need for multicore SoC for getting high performance while keeping the power density and design effort manageable. We will consider some case studies for multicore SoC in application areas such as video processing. (1.5 hrs)
- Power Management in Modern-day SoC – Unless power management strategies are adopted in modern-day SoC that pack billions of transistors and operate at high clock frequencies, the power density will be intolerable. In this section, we will look at some solutions to the power management problem. We will look at aspects of energy management, battery management, and energy harvesting. (1.5 hrs)
- Challenges in VLSI Test – Need for BIST to meet ITRS goal, compaction and compression of test data, diagnosis issues, and power/thermal aware test scheduling. (2 hrs)

C.P. Ravikumar is presently the Technical Director of University Relations at Texas Instruments, India. He also leads the TI India Technical University, which provides learning opportunities to employees of TI India. He is also an adjunct faculty at IIT Madras. Before joining TI India in 2001, Ravikumar was a Professor of Electrical Engineering at the Indian Institute of Technology, Delhi (1991-2001). He also held a visiting position at the University of Southern California (1995-1996) and the position of Vice President (Training) at Controlnet India Pvt Ltd (2000-2001). He obtained his Ph.D. (Computer Engineering) from the University of Southern California (1991), M.E. in Computer Science with highest scores from Indian Institute of Science (1987) and B.E. in Electronics with a Gold Medal from Bangalore University (1983).
He has published over 200 papers in leading International conferences and journals. He founded the VLSI Design and Test Symposium (VDAT) and has been the General Chair of this event from its inception in 1998. He is the author/editor/coauthor of over 12 books in areas of VLSI. He has won the best paper award at IEEE International Conference on VLSI Design (2002) and VLSI Test Symposium (2005). He is a Senior Member of IEEE and the honorary secretary of VSI.

<table>
<tr><th colspan="4">July 8, 2011 (Friday)</th></tr>
<tr><td>08.00 AM - 09.00 AM</td><td colspan="3">Registration and Breakfast</td></tr>
<tr><td>09.00 AM - 09.30 AM</td><td colspan="3">Inauguration
Venue: Room A</td></tr>
<tr><td>09.30 AM - 11.30 AM</td><td colspan="3">Session 2A-1: Keynote Sessioin-1
Embedded Microcontroller Solutions for Automobile Safety
Hoiman Low (Texas Instruments)
Keynote Talk-2
Convergence of Bio-Nano-Information Technologies in the Nanoelectronics Era
V.Ramgopal Rao (Institute Chair Professor, EE Department, IIT Bombay)
Chair: TBA
Venue: Room A</td></tr>
<tr><td>11.30 AM - 11.45 AM</td><td colspan="3">Tea Break</td></tr>
<tr><td rowspan="3">11.45 AM - 12.45 PM</td><td>Session 2A-2
Analog-1
Chair: Subhajit Sen (DAIICT, Gandhinagar)
Venue: Room A</td><td>Session 2B-2
Memory-1
Chair: TBA
Venue: Room B</td><td>Session 2C-2
Low-power
Chair: Vishwani D.Agrawal (Auburn University)
Venue: Room C</td></tr>
<tr><td>A Novel Fully Differential Folded Cascode Operational Transconductance Amplifier
Kumaravel Sundaram, Venkataramani Balasubramanian; Ajit Randhir; and Ramakrishna Chowtri (NIT Trichy)
49 (Regular Paper)</td><td>BER Analysis of Flip-Flop and Latches with Wire Pipelining
Devendra Giri; Gagnesh Kumar; and Diwakar Singh (NIT Hamirpur)
102 (Regular Paper)</td><td>A Method to Reduce Switch-on Delay in Miller Based Slew Rate Controlled IO
Dharmaray Mallappa Nedalgi; and Kiran Gopal (NXP Semiconductors)
100 (Short Paper)</td></tr>
<tr><td>Inductive Degenerated Low noise Amplifier for Wireless Application in 0.18um UMC CMOS
Kapil Soni; and Rajendra M.Patrikar (VNIT, Nagpur)
66 (Regular Paper)</td><td>Tied-Gate DG-FinFET based Radiation Tolerant SRAM Cells
Surendra S.Rathod; A.K. Saxena; and S Dasgupta (IIT Roorkee)
4 (Short Paper)</td><td>Architectural Power Management for Battery Lifetime Optimization in Portable Systems
Manish Kulkarni; and Vishwani D.Agrawal (Auburn University)
108 (Embedded Tutorial (40 min))</td></tr>
<tr><td>12.45 PM - 01.45 PM</td><td colspan="3">Lunch</td></tr>
<tr><td rowspan="4">01.45 PM - 03.45 PM</td><td>Session 2A-3
Analog-2
Chair: Chetan D.Parikh (DAIICT, Gandhinagar)
Venue: Room A</td><td>Session 2B-3
Memory-2
Chair: H.C.Srinivasaiah (DayanandaSagar College of Engg)
Venue: Room B</td><td>Session 2C-3
Verification
Chair: TBA
Venue: Room C</td></tr>
<tr><td>A Low Glitch Current Switch with Reduced Swing and its Application to PLL Charge Pump
Subhajit Sen (DAIICT, Gandhinagar); and Amir Hadji-Abdolhamid (Broadcom, Irvine, USA)
2 (Regular Paper)</td><td>Critical Charge Model for Novel Radiation Tolerant Flip-Flop
Surendra S.Rathod; A.K. Saxena; and S Dasgupta (IIT Roorkee)
3 (Regular Paper)</td><td>Foolproof Methodology to Verify Clock stop in SoC
Narendran Kumaragurunathan (AMD)
105 (Regular Paper)</td></tr>
<tr><td>Low Voltage Constant Hysteresis Schmitt Triggers
Jayarama Ubaradka (NXP Semiconductors)
19 (Regular Paper)</td><td>A (1/5.5 x VDD) to (3/2 x VDD) Bidirectional I/O Buffer at 0.35µm, 3.3V CMOS Technology using Innovative Input Receiver
Arnab Biswas; and S Dasgupta (IIT Roorkee)
63 (Regular Paper)</td><td>Simulation of Low Voltage Flash Memory Cell
Ashwini Shrirao; Rashmi Gautam; and Rajendra M.Patrikar (VNIT, Nagpur)
73 (Regular Paper)</td></tr>
<tr><td>Design and Analysis of Low Noise Amplifier for WiMAX application
Suresh Naidu Lekkala; and Bhuvan B (NIT Calicut)
44 (Regular Paper)</td><td>Self Times System Design using FIFO
Mansi Jhamb (USIT, GGSIPU); Vinod Kumar Khera (GTBIT, GGSIPU); R.K. Sharma; and A.K. Gupta (NIT Kurukshetra)
96 (Short Paper)

Halo Implant Photoresist Mask layer Shadow effect on Leakage in 65nm SRAM Cell
H.C. Srinivasaiah (DayanandaSagar College of Engg)
53 (Short Paper)</td><td>CATD: A Tool for Consistency Analysis of Timing Diagrams
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45 (Short Paper)

Layered Testbench Framework for Verification
Praveen Kumar K. (Intel Mobile Communications)
34 (Embedded Tutorial (40 min))</td></tr>
<tr><td>Optimized Flash Analog to Digital Converter using LCT Comparator
Meghana Kulkarni (K.L.S. G.I.T. Belgaum); V Sridhar (P.E.S. College of Engineering, Mandya, Karnataka); and G. Kulkarni (Jain College of Engineering, Belgaum, Karnataka)
18 (Short Paper)</td></tr>
<tr><td>03.45 PM - 04.00 PM</td><td colspan="3">Tea Break</td></tr>
</table>

July 8 Continued

03.45 PM - 04.00 PM	Tea Break		
04.00 PM - 05.00 PM	**Session 2A-4** **Analog-3** **Chair: Hitesh Garg** (NXP Semiconductors) **Venue: Room A**	**Session 2B-4** **FPGA** **Chair:** TBA **Venue: Room B**	**Session 2C-4** **Research Scholars' Forum - 1** **Chair: Dipankar Nagchoudhuri** (DAIICT, Gandhinagar) **Venue: Room C**
	A 110-MHz Rail-to-rail Amplifier with Double-gate MOSFETs **Chetan D.Parikh** (DAIICT, Gandhinagar); and Amara Amara (ISEP, France) 38 (Short Paper)	**VLSI Architecture and FPGA Implementation of Image Enhancement Algorithms** **Hitendra Gupta** (LNMIIT, Jaipur); Kamlesh K.Sharma (MNIT, Jaipur); and Shiv D.Joshi (IIT Delhi) 1 (Regular Paper)	**Performance Optimization of FinFET for Ultralow Power Circuits** **Sachin D.Pable** (PDVVP's COE Ahmednagar) 11 **On-Line Detection of Crosstalk Fault in FPGA Using BIST model** **Nachiketa Das** (BESU, Shibpur) 59 **Design of RFLow Noise Amplifier using CMOS Technology at 2.45GHz** **Anand S.Deshkar** (G.H.Raisoni College of Engg) 93
	Automating the Design of Successive Approximation Analog to Digital Converters **Purushothaman A**; and Chetan D.Parikh (DAIICT, Gandhinagar) 40 (Regular Paper)	**Development of a Bird's eye view Parking Assistance System on a Programmable Multimedia Processor** **Bijo Thomas**; Yann Picard; Rajiv Chithambaran; and Cecile Cougnard (NXP Semiconductors) 58 (Regular Paper)	
End of Day-2			

July 9

July 9, 2011 (Saturday) – Day-3			
08.00 AM - 09.30 AM	Registration and Breakfast		
09.30 AM - 10.30 AM	**Session 3A-1: Keynote Sessioin-2** **Automotive Electronics Innovation Driven by global trends and challenges for Society** **Carol de Vries** (Vice President, R&D, Business unit Automotive of NXP Semiconductors) **Chair: TBA** **Venue: Room A**		
10.30 AM - 11.00 PM	Tea Break		
11.00 AM - 01.00 PM	**Session 3A-2** **Physical Design** **Chair:** TBA **Venue: Room A**	**Session 3B-2** **Devices** **Chair: N.S.Murty** (NXP Semiconductors) **Venue: Room B**	**Session 3C-2** **Research Scholars' Forum - 2** **Chair: C.P. Ravikumar** (TI India) **Venue: Room C**
	Low Power High Throughput Differential Current Mode Signaling Technique for Global VLSI Interconnect **Sujeet Kumar**; R.B. Deshmukh; and Rajendra M.Patrikar (VNIT, Nagpur) 78 (Regular Paper)	**3.3-V Signaling with 2.5-V Devices using Dynamic Biasing** **Jayarama Ubaradka**; and Dharmaray Nedalgi (NXP Semiconductors) 10 (Short Paper)	**Investigation of Linearity Performance of a Double Gate Band to Band Tunnel Field Effect Transistor** **Rakhi Narang** (University of Delhi) 25
	Cluster based Routing for Multi pin droplets in Digital Microfluidic Biochips with Intelligent Collision Avoidance **Pranab Roy**; Hafizur Rahaman (B.E.S.U, Shibpur); and Parthasarathi Dasgupta (I.I.M, Calcutta) 46 (Regular Paper)	**Simulation of 22nm n-Metal Oxide Semiconductor Field Effect Transistor** **Madhuri Borkar**; Rashmi Gautam; and Rajendra M.Patrikar (VNIT, Nagpur) 74 (Short Paper)	**Analog Performance of Insulated Shallow Extension Silicon On Nothing (ISE-SON) MOSFET: Simulation study** **Vandana Kumari** (University of Delhi) 26
	On-Chip Test Circuits for Throughput Measurement of High Speed Interconnects **Amit J. Vishnani**; Marshnil V. Dave; Maryam S. Baghini; and Dinesh K. Sharma (IIT Bombay) 91 (Regular Paper)	**A Design of Experiment based Approach to Variance Optimal Design of Analog Circuits** **Arnab Khawas**; Siddhartha Mukhopadhyay (IIT Kharagpur); and Amitava Banerjee (National Semiconductor) 17 (Regular Paper)	**A Wide Temperature Range (50-500K) Analysis For Nanoscale Surrounding Cylindrical Gate MOSFET With Localised Charges** **Rajni Gautam** (University of Delhi) 27
			Study of Energy Efficiency of Single Phase Energy Recovery Logic with Progressive Technology **Jitendra Kanungo** (IIT Roorkee) 77
			Analysis and Modeling of Series Resistance in SI-Nanowire MOSFET **Gaurav Kushal** (IIT Roorkee) 92
			Low power Switching Activity on Scan based Testing Vector using Folding Method **Saravanan Sivasankaran** (SASTRA University, Tanjore) 99
			Behavioural Analysis of Clock Jitter Effects in Continuous Time Sigma Delta Modulator **Kumaravel Sundaram** (NIT Trichy) 51
01.00 PM - 02.00 PM	Lunch		
02.00 PM - 03.00 PM	**Session 3A-3** **Wireless** **Chair: Rajnish Sharma** (CIET, Chandigarh) **Venue: Room A**	**Session 3B-3** **Automotive** **Chair:** TBA **Venue: Room B**	**Session 3C-3** **Verification-2** **Chair:** TBA **Venue: Room C**
	Wireless System Design and System Engineering Challenges Muralidhar Bandi; Kameswara Rao B; Ajith Kumar V K; and **B. Ravi Kishore** (HCL Technologies) (Short Tutorial)	**Integrated Chip Quality For Automotive Applications** **Raghavendra Dattatraya**; Jagadeesh Nallagatla; and Poornima Prahlada (NXP Semiconductors) (Short Tutorial)	**Design and Verification with SystemC** **Bhanu Kapoor** (Mimasic), Prapanna Tiwari (Synopsys), Shireesh Verma (Conexant), and Rahul Joshi (Chip Design Pvt. Ltd., Gurgaon) (Short Tutorial)
03.00 PM - 03.15 PM	Tea Break		

July 9 Continued

<table>
<tr><td>03.00 PM - 03.15 PM</td><td colspan="3">Tea Break</td></tr>
<tr><td rowspan="4">03.15 PM - 04.15 PM</td><td>Session 3A-4
Nanotechnology
Chair: TBA
Venue: Room A</td><td>Session 3B-4
Architecture
Chair: Sheetal Bhandari (I2IT, Pune)
Venue: Room B</td><td>Session 3C-4
VSI Meeting
Chair: C.P. Ravikumar (TI India)
Venue: Room C</td></tr>
<tr><td>Invited talk
TBA</td><td>Implementation of Embedded Resizing for MPEG-2 Decoder on Trimedia
Dayananda KS; and Milind Sureshrao Phadtare (NXP Semiconductors)
86 (Regular Paper)</td><td rowspan="3">VLSI Society of India will host a meeting where participants from the industry and academia can come face to face to discuss problems and solutions. If you wish to make a formal presentation, please send e-mail to C.P. Ravikumar (ravikumar@vlsi-india.org)</td></tr>
<tr><td>Optimisation of Lateral Silicon Nanowire based Solar Cell using 3D TCAD Simulation
Jitendra Kumar; Sanjeev K.Manhas; Brijesh K.Kaushik; A.K. Saxena; and Dharmendra Singh (IIT Roorke)
88 (Short Paper)</td><td rowspan="2">Design and Implementation of Differential Serial Interconnect using Wave pipelining and Surfing
Bhaskar Manickam; Parthiban Dhanapal; and Venkataramani Balasubramanian (NIT Trichy)
52 (Short Paper)</td></tr>
<tr><td>Performance Analysis of Carbon Nanotube Interconnects
Tafseer Alam; Rohit Dhiman; and Rajeevan Chandel (NIT Hamirpur)
70 (Short Paper)</td></tr>
<tr><td>04.15 PM - 04.30 PM</td><td colspan="3">Break</td></tr>
<tr><td>04.30 PM - 05.30 PM</td><td colspan="3">Session 3A-5: Panel Discussion
VLSI Education in India: What is the next step?
Moderator: Prof. Vishwani D. Agrawal (Auburn University)
Panelists: Dipankar Nagchoudhuri (DAIICT, Gandhinagar), Rajnish Sharma (CIET, Chandigarh), and N.S. Murty (NXP Semiconductors)
Venue: Room A</td></tr>
<tr><td>05.30 PM - 06.00 PM</td><td colspan="3">Session 3A-6
Valedictory
Venue: Room A</td></tr>
<tr><td colspan="4">End of Symposium</td></tr>
</table>

Panel Discussion: VLSI Education in India: What is the next step?

It has been more than 50 years since the introduction of the IC. Moore's law has enjoyed an unparalleled reign of over 4 decades, fuelled by innovations in devices, manufacturing technology, EDA, and design methodologies. Today, the field of semiconductors has matured and innovations are more infrequent. Some people believe that alternate technologies such as nanotechnology will be the future. VLSI Design was introduced in Indian education about two decades ago. Today, the topic of VLSI is covered in almost every undergraduate curriculum in Electronics. There are many M.Tech. Programs in VLSI design in the country. In this panel discussion, the panelists will discuss

1. Are India's needs in VLSI education different from those of other countries e.g. USA/Europe/China? Does our curriculum reflect our needs?
2. Going forward, what topics related to VLSI must be introduced and what topics must be removed in a UG course to make it more relevant.
3. Going forward, what topics related to VLSI must be introduced and what topics must be removed in a PG course to make it more relevant.
4. How can industry and academia co-define a new curriculum for VLSI in the country?

Keynote Talk-1: Embedded Microcontroller Solutions for Automobile Safety (**Hoiman Low**, Texas Instruments)

Abstract: The use of microcontrollers in automobile safety applications such as Anti-Lock Brake System (ABS), Electronic Stability Program (ESP) and Airbag System have grown significantly in recent years. These are 32-bit CPU microcontrollers designed in sub-micron embedded Flash technology. The expectation is that these microcontrollers work reliably under harsh environmental conditions over the full life time. This presentation examines the design options to address 0 dppm quality, safety goal and system availability target.

Speaker bio: Hoiman Low is the Automotive MCU Design Manager at Texas Instruments. He is responsible for all the TI Automotive MCU designs for safety applications. These MCUs are used in the majority of the worldwide automobile braking ECU such as ABS and ESP controllers. He graduated from Imperial College, University of London with a Physics degree. He has been employed at TI since 1983 in various capacities, such as product engineering, application, program management and design, and embedded Flash development.

Keynote Talk-2: Convergence of Bio-Nano-Information Technologies in the Nanoelectronics Era (**V.Ramgopal Rao,** IIT Bombay)

Abstract: CMOS scaling is expected to slow down owing to the huge cost, power and variability constraints. This has necessitated a paradigm shift in the CMOS scaling trends from the “More Moore” to the “More than Moore”, allowing for the integration of heterogeneous technologies on a CMOS platform. The key idea is to achieve a functional diversification on the chip by empowering the CMOS technologies with a variety of “sense & interact” functions. In this talk we will look at the nano-electro-mechanical-systems (NEMS) as one such enabling platform for sensor integration with the CMOS.

Many of the bio-chemical sensing applications require an ultra sensitive, low cost and disposable sensor. In this work we present a novel polymer process technology for realization of a highly sensitive nano-particle based piezo-resistive polymer composite cantilevers that can be fabricated at sub 100^{o} C process temperatures, allowing for the integration of these technologies on a CMOS die. Electro-mechanical characterization of the fabricated microcantilevers yielded a resonance frequency, which is a few tens of kHz and a deflection sensitivity in the range of 1 ppm ($\Delta R/R$) for a nanometer of deflection. These cantilevers have been used for a range of applications such as for detection of explosive molecules such as TNT/RDX in the parts-per-trillion level of concentrations as well as for developing an integrated system to provide point-of-care diagnostic support for cardiovascular diseases. Prototypes of these systems are currently under development at IIT Bombay for field trials. *These activities involve collaborations between faculty & students from the Departments of Electrical Engg., Bio Sci. & Engg, Metallurgy & Materials Science, Physics, Chemistry, Mechanical Engineering, and Industrial Design Centre at IIT Bombay.*

A company NanoSniff Technologies Pvt. Ltd. is incubated at IIT Bombay for commercialization of these technologies.

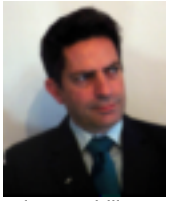
Speaker bio: Dr. V. Ramgopal Rao is an Institute Chair Professor in the Department of Electrical Engineering, IIT Bombay and the Chief Investigator for the Centre of Excellence in Nanoelectronics project at IIT Bombay. Dr. Rao has over 280 publications in the area of Electron Devices & Nanoelectronics in refereed international journals and conference proceedings and has 15 patents, either awarded or pending.

Prof. Rao received the coveted **Shanti Swarup Bhatnagar** Prize in Engineering Sciences awarded by the Hon'ble Prime Minister, Govt of India in 2005 for his work on Electron Devices. He is also a recipient of the 2004 **Swarnajayanti** Fellowship award from DST, 2007 IBM Faculty award, the 2008 MRSI-ICSC Annual Prize, the 2009 Techno-Mentor award from the Indian Semiconductor Association and the 2010 DAE-SRC Outstanding Research Investigator award. He is an Editor for the IEEE Transactions on Electron Devices in the CMOS Devices and Technology area and serves on the Editorial boards of various other international journals. Dr. Rao is a Fellow of the Indian National Academy of Engineering, a Fellow of the Indian Academy of Sciences, a Fellow of the National Academy of Sciences and a Fellow of IETE. He is a Distinguished Lecturer, IEEE Electron Devices Society and interacts closely with many semiconductor industries including Intel, IBM, Infineon, Applied Materials and Texas Instruments. He has served on the program/organizing committees of a large number of international conferences in the area of electron devices and was Chairman, IEEE AP/ED Bombay Chapter during 2002-2003. He currently serves on the executive committee of the IEEE Bombay Section besides being the vice-chair, IEEE Asia-Pacific Regions/Chapters Subcommittee.

For more information about Prof. Rao’s current research interests and a list of publications visit: http://www.ee.iitb.ac.in/~rrao/

Keynote Talk-3: Automotive Electronics Innovation Driven by Global trends and Challenges for Society (**Carol de Vries,** NXP)

Abstract: Seamless Connectivity, Sustainable mobility, Increased Safety and Comfort and Affordability are the main drivers of innovation in automotive electronics industry. All the challenges give a new focus to the semiconductor industry requiring high performance mixed signal solutions. These challenges are also driven by local needs around the globe and provide immense innovation opportunities. In this keynote, Carol will bring out the trends and challenges and throw light on how the innovations in VLSI and embedded systems domains are enabling automotive industry meeting the challenges.



Speaker bio: In his current position (VP Research and Development), **Carol de Vries** is responsible for all R&D activities in the Business Unit Automotive of NXP, one of 4 Business Units, with currently 6 Business lines and 6 new business activities. He drives operational excellence in R&D, making sure their execution and PCP processes are world class with continuous improvement. He is driving competitive technology and product roadmaps and advanced Innovation and Research activities, and has a strong focus on discovery and guiding new business activities to success. He is part of the NXP R&D leadership team, which looks at long-term strategies and Research direction. He has more than 28 years of experience in the electronics industry.

With a background in Physics, he started his career in Philips Research on new process technologies for IC's in 1982. As part of a large Philips project, he became responsible first for setting up a submicron development and production line, and later ran it as Operations manager in 1985. This was later extended with the business responsibility for CCD image sensors for professional applications.

In 1994 he moved to Philips Components, first to reorganize and run development and new business creation for the business unit Passive Components. Later, he did a similar job as CTO bringing a number of power module and component related businesses together and making them profitable. For both businesses he was part of the divestment team as they were later sold to third parties.

Within Philips Components, he then helped to set up a new strategy and develop new business, working on LCD TV, Hard Disk recording and wireless communication modules. When this was moved to Philips Consumer Electronics in 2003, he returned to Philip Semiconductors first to set up program management for deep submicron processes (from 120nm to 65nm) and help streamline the central organization. Before finally moving to his current BU position in 2006, he also ran the central advanced application labs and the central System and Architecture organization. He is one of the founding members of the NXP management when split off from Philips.

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ravikumar@vlsi-india.org

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Treasurer, VLSI Society of India
Finance Chair (VDAT 2011)
Texas Instruments (India) Pvt Ltd
Bagmane Tech Park, Opp. LRDE
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Ph: 080 – 25099362; Fax: 91 - 080 - 25099717
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Since the symposium venue is the campus of *Wipro Technologies*, we need to work with the Security personnel of *Wipro* to make the process of entering the campus and registering a smooth one. Please follow the rules and regulations given below. Your cooperation in this regard is appreciated.

Please bring your original photo ID Card (a valid company/college ID card with your photograph). *Wipro* security personnel are instructed to allow entry only to the participants who have their valid proof of identity.

For the registered participants, the ***VDAT2011*** ID badge will be provided, after presenting a valid photo ID card. Please wear your *VDAT2011* ID badge throughout the duration of the workshop.

Please notify spot registrations in advance by filling the online registration form on VDAT2011 website.

During entry/exit to the campus, the physical security team at *Wipro* might frisk you, and/or ask to declare your belongings. Please cooperate with them.

Please declare all media (magnetic/CD/flashdrive) and/or laptop at Wipro security office (main gate) while entering the campus.

Please do not smoke at the venue (except in designated areas). Thanks for your cooperation.

In addition to lunch/tea served during breaks, you can purchase breakfast and dinner at the cafeteria on all the days.

Registration Information:

- Registration permits you to participate in all the Technical sessions and Tutorials organized as part of the Symposium, and includes refreshments and lunch on all days.
- Tutorials and Symposium needs separate registration. A common payment for both is preferred. If applying separately, please repeat the regn process for each.
- Please send your registration fee through a Demand Draft (DD) made out to **VLSI Society of India**, payable at Bangalore**.** Follow the before/ after deadline rate. If the DD is made out on or before the deadline, and reaches us slightly late, it would be considered as before-deadline registration.
- The draft must be sent to ***Mr. Dinesh Bapat,*** *Finance Chair (VDAT 2011), Texas Instruments India, Bagmane Tech Park, C.V. Raman Nagar, Bangalore 560093.*
- If you wish to register *on the spot*, drafts and cash payment in Indian rupees are acceptable. We will not be able to accept Credit Card payments.
- The current exchange rate is approximately 1 US dollar = 50 Indian rupees.
- Even those of you who plan to register on the spot are requested to communicate your desire to attend VDAT 2011 through online form. Details of vehicle registration number (if any) and laptop number (if any) should be sent to vdat-local@vlsi-india.org with a copy to vdat@vlsi-india.org. Without this, you may face difficulties during registration.
- If you are registering for a tutorial, indicate the first and second preference of the tutorial. There are limited seats in each tutorial. If we cannot register you in the tutorial of your choice, we will refund the amount.
- A processing fee of Rs 500/- will be applied against all cancellations.
- **Bulk Registration:** We will offer **one** complimentary registration for every **five** registrations received from the same organization. All the **six** names should be registered with full information quoting the same DD details. Authors of accepted papers may also be included.
- Visit VDAT2011 website for updates on Accommodation and travel.

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Category	**Member**	**Non-member**	**Member**	**Non-member**
Students	Rs 1000/-	Rs 1250/-	Rs 1250/-	Rs 1500/-
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Indian Industry Participants	Rs 2000/-	Rs. 2500/-	Rs 2500/-	Rs 3000/-
Foreign Participants	USD 50	USD 75	USD 75	USD 100

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Faculty Members and Government R&D	Rs 2000/-	Rs 2500/-	Rs. 2500/-	Rs. 3000/-
Indian Industry Participants	Rs 4000/-	Rs 4500/-	Rs. 4500/-	Rs. 5000/-
Foreign Participants	USD 75	USD 100	USD 100	USD 150

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- ✓ Government-issued ID card such as passport/Driver's license
- ✓ Student ID card (for student participants)
- ✓ You will be required to provide your contact phone number and address at the security booth.

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1st VDAT	Chennai	January 7, 1998	30
2nd VDAT	New Delhi	August 6-7, 1998	70
3rd VDAT	New Delhi	August 20-21, 1999	120
4th VDAT	New Delhi	August 25-26, 2000	150
5th VDAT	Bangalore	August 16-18, 2001	220
6th VDAT	Bangalore	August 29-31, 2002	300
7th VDAT	Bangalore	August 28-30, 2003	300
8th VDAT	Mysore	August 26-28, 2004	250
9th VDAT	Bangalore	August 10-13, 2005	350
10h VDAT	Goa	August 9-12, 2006	250
11th VDAT	Kolkata	August 8-11, 2007	250
12th VDAT	Bangalore	July 23-26, 2008	200
13th VDAT	Bangalore	July 8-10, 2009	250
14th VDAT	Himachal Pradesh	July 8-10, 2010	200

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VDAT 2011

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Payment Details	Towards Tutorial		DD Number	
	Towards Symposium		Dated	
	Total Amount		Bank	

Which of the days do you wish to attend? (Tick appropriate)

T1 only ☐ **T2** only ☐ **T3** only ☐

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Signature

Tutorial Registration Amount

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Students	Rs. 1000	Rs 1250	Rs. 1250	Rs 1500
Faculty Members and Government R&D	Rs. 1000	Rs 1250	Rs. 1250	Rs.1500
Indian Industry Participants	Rs. 2000	Rs.2500	Rs. 2500	Rs 3000
Foreign Participants	USD 50	USD 75	USD 75	USD 100

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Indian Industry Participants	Rs 4000	Rs. 4500	Rs. 4500	Rs. 5000
Foreign Participants	USD 75	USD 100	USD 100	USD 150

Member indicates VLSI Society of India or IEEE member

Mail the completed registration form and DD to the following address:

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Treasurer, VLSI Society of India
Finance Department
Texas Instruments (India) Pvt Ltd
Bagmane Tech Park
C.V. Raman Nagar, Bangalore 560093
Phone: 080-2509 9362
FAX: 2509 9717
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- The DD to be made out to "**VLSI Society of India**" payable at **Bangalore, India**. On the rear side of DD, please write **Towards VDAT2011** (Symposium/Tutorial/Symposium+Tutorial as applicable).
- The DD and form to be sent to the VDAT2011 Finance Chair, at the address mentioned.
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Please watch the VDAT website or follow the VDAT Yahoo group mailing list for any updates to the program. Since the space for tutorials is limited, we may be forced to shortlist participants. If we are unable to register you, you will be intimated by e-mail, and a refund will be made by the VLSI Society of India. Watch VDAT2011 website for general updates.

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Place and Date: **Member Signature**

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