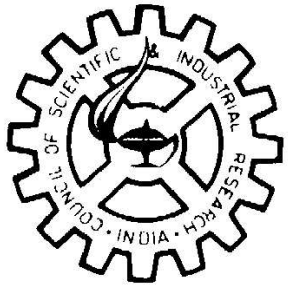
VLSI Education in India :

Towards Excellence, Numbers and Relevance

Presenter : Chandra Shekhar



IC Design Group
CEERI
Pilani – 333 031
(Rajasthan)

Phone : 01596-242359
FAX : 01596-242294
Email : chandra@ceeri.ernet.in

VLSI Education and R&D : Indian Mile-Stones

1979-80

Start of VLSI Education in India with the publication of the path-breaking book, *Introduction to VLSI System Design* by Mead and Conway in 1980, and the introduction of “VLSI Design” courses based on it by some IITs.

Adoption of the book’s methodology by TIFR and CEERI for their design R&D work.

Concurrently, MOS technology development related R&D work was being pursued at TIFR, CEERI and IITs.

1980-81

Setting up of SCL and the “VLSI Task Force” by Government of India. Big hopes! Big proposals and investment recommendations! Only realistic follow-ups.

1981-82

First commercial interactive layout design system (among academic and R&D institutes) installed at CEERI’s Delhi Centre under UNDP support – An Applicon System.

Mid 1980s

Evolution of more focused integrated electronics and circuits oriented ME/MTech degree programmes at IITs.

1985-86

First multinational company, TI, sets up its R&D Centre in India (for EDA tool development and software verification).

1986-87

First real application of Mead-Conway methodology to design a full custom LSI processor — the PWM processor for variable frequency AC drives at CEERI, Pilani together with UCL, Belgium (under UNDP support).

1987-88

Setting up of Academic and R&D VLSI Design Centres at IITs and CEERI under a major initiative of the then Department of Electronics (DoE), Government of India.

Academic Centres were equipped with Sun workstations and VTI tools (an integrated tool-set for full-custom and semi-custom logic, circuit and layout design and verification) and the indigenous semi-custom design tool “Vinyas” developed by ITI that ran on a particular brand of PC (the OMC PC-286 and PC-386).

Along side these academic-R&D centres, 10 industrial VLSI Design Centres were also set up by DoE — 5 under the charge of SCL and 5 under the charge of ITI.

Development of PLA-based FSM compiler at CEERI, Pilani.

Development of a high-level synthesis tool under the Rachana project at IIT-Delhi.

Start of VLSI Design Workshop and International Conference.

Early 1990s

Successful chip design-developments by academic-R&D design centres :

CEERI (for C-DoT) using VTI tools and VTI foundry.

IIT-Kharagpur and Jadavpur University using Vinyas tools and ITI foundry.

1994

Introduction of VHDL in the Indian academia and R&D — adoption of VHDL for modeling and simulation of a micro-processor design by CEERI, Pilani.

1997

Start of the first industry-sponsored MTech programme — “VLSI Design, Tools and Technologies” (VDTT) programme at IIT-Delhi sponsored by Philips and co-sponsored by a number of other industries.

Subsequently, TCS has supported a MTech degree programme at IIT-Bombay.

1998 onwards

Major government initiative in VLSI education via DoE/MIT project, Special Manpower Development for VLSI Design and Related Software (SMDP), based on industrial and academic inputs for the 9^{th} plan.

The project has 7 Resource Centres (RCs) and 12 Participating Institutes (PIs).

RCs : IIT-Bombay, IIT-Delhi, IIT-Kanpur, IIT-Kharagpur, IIT-Madras, IISc-Bangalore and CEERI-Pilani.

PIs : NITs at Warangal, Surathkal, Rourkela, Nagpur, Jaipur; IIT-Roorkee, IT-BHU, TIET-Patiala, PSGCT-Coimbatore, BEC-Howrah, SGSITS-Indore and Jadavpur University, Kolkata.

Activities Under SMDP

Furnishing of labs with Books, Workstations and PCs.

Provision of CAD tools : Cadence, Synopsys, Model Tech, Tanner, Xilinx, Saber.

16 different Instruction Enhancement Programmes (IEP) of 2-3 weeks duration by RCs for the faculty members of PIs and RCs.

Development of Learning Material (LM) on 25 different VLSI related subjects including 8 Laboratory Learning Materials.

Objectives of SMDP

To start and strengthen ME/MTech (VLSI Design / Microelectronics) programmes at PIs to generate 250-300 such specialized graduate manpower annually. These are called Type-II manpower.

To expose the ME/MTech students of other electronics disciplines (communications, control, ...) to at least two relevant VLSI courses. Manpower so trained is termed Type-III manpower.

To expose under-graduate (BE/BTech) students of EE/ECE/CS to two basic VLSI design courses. This is Type-IV manpower.

To promote PhD in Microelectronics, called Type-I manpower.

Corporate Initiatives in VLSI Education

More than 10 public and private sector corporates are involved in providing 4-6 months diplomas in VLSI Design.

VLSI Design Industry : Indian Mile-Stones

1989

TI starts IC design and library related work. Arcus and SASI initiate VLSI design related operations. EDA tool vendors set up support offices.

1991 onwards

Many MNCs start captive design centres. EDA tools companies start software development centres. Many IC/VLSI design services companies start operations.

Current Academic Status

Institutes offering ME/MTech degree in VLSI/Microelectronics discipline are the 6 (IITs and IISc) + 10 (NITs and Other) Institutes.

Total Core Faculty Pool Size	:	60-70
Graduating Type-II Manpower/year	:	250-300
Graduating Type-III Manpower/year	:	150-200
Graduating Type-IV Manpower/year	:	1,000-1,200
Graduating Type-I Manpower/year	:	8-12

Future Perspective

TCS+IIT-Bombay Report has projected a need for about **4,000 ME/MTech** per year in VLSI/Embedded System Design.

Requirements for generating **1,000 ME/MTech** per year :

Required number of institutes	:	50-60
Required Faculty Pool size	:	250-300
VLSI Lab. Set-up	:	Rs. 50-60 Crore
Books, Journals, . . .	:	Rs. 8-10 Crore
Scholarships/Self-finance	:	For 2,000 Students

Bottle-necks

Faculty pool size and its growth from the current level of 60-70 to desired level of 250-300 over the next 3 years.

ME/MTech thesis supervision.

Funding of tools for deployment in numbers.

Silicon access (technical and financial support).

Possible Solutions

Use of technology (dedicated multimedia links via Internet / TV) for live broadcasts of lectures to partially alleviate the faculty short-fall in the immediate future as vigorous faculty-development proceeds side-by-side.

Electronic availability of lecture/learning/course materials.

Industry to pitch-in with their senior engineer / project leader level manpower as guest faculty (out of conviction and with full-support of their top-level management).

Industry (private and public-sector) and government R&D centres (DRDO, ISRO, CSIR, DAE) to very significantly increase their in-take of ME/MTech thesis students.

Problems Faced by Academic Labs

Course Labs

Costs associated with the deployment of Hardware-Software in large numbers.

Time needed to get started with the tools.

Insufficient technical support.

Suggestions

Use public-domain / cheaper / simpler commercial tools.

Select senior students (with aptitude) as lab instructors. They are better hands-on as compared to senior faculty. They also set up a relaying mechanism from batch-to-batch.

Problems Faced by Academic Labs

Project Labs

Problems of installation, commissioning, periodic updating and technical support for professionally-used tools.

Long times involved in taming the tool — learning how to use the tool (or the design environment and flows) and its features effectively to express one's design concepts and proceed with the design.

Maintenance and upkeep of hardware items.

Infrastructure support problems (UPS, Air-conditioning, . . .).

Problems Faced by Academic Labs

Suggestions

Appoint Laboratory Engineers whose defined job is to tame the tool (with conceptual inputs from the faculty).

They should set up demos for the students on how to effectively use the tool and answer their specific queries related to the tool-features and its capabilities.

The lab engineers would also initially hand-hold the students in their tool usage.

New Courses Needed

RF IC Design and Test.

Mixed-Signal Design and Test.

VLSI-SoC System Architecting : that takes a unified view of logic design and its optimization across hardware-software boundary to obtain the required speed-power-cost-design-time trade-offs offered by different approaches.

VLSI (and SoC) Test and Testability : too little attention has been paid to it in academics.

Low-Power Design : circuit techniques, logic styles, dynamic voltage scaling, dynamic power management, low-power system and micro-architecting, low-power codes and compilers.

New Courses Needed

Memory Design and Memory Subsystem Design.

Sensors, MEMS, Signal Conditioning and Interface Circuits.

Signal Processing and Architectures for Speech / Audio / Video / Image / Multimedia Applications.

Courses on New and Evolving Standards in Different Applications Areas (with a bearing on VLSI-SoC Architectures).

Strengthening of Research

Research is the bedrock of any good graduate programme. Research needs to be recognized as an essentiality for maintaining quality and relevance.

New areas, new courses, new topics, new examples, emphasis and clarity are born out of research only.

Special interest groups on particular research areas/topics that can tightly interact via the Net and meetings need to be formed to provide the necessary impetus and the supportive human environments required for good research. This would help to set up research communities among the academic and R&D institutes.

Strengthening of Research

Need to network the researchers and their available knowledge for a larger technology demonstration projects for one or more application areas.

This effort should also provide case-study material for large system designs which can be used as examples in post-graduate programmes. This would provide the graduate students a peek into large real-life projects thus bridging the gap between class-room examples and industrial practices.

VLSI Challenges : Evolution of VLSI Design Scenario

Year	Team Size (At Peak)	Effort (Man-Years)	Nature of Product	MDI*
1985	2–3	3–5	ASICs for Glue Logic	0.2
1990	10–12	10–15	ASP, Chip-sets	0.4
1995	30–50	30–50	ASP, Analog, Mixed-Signal	0.7
2000	100–200	100–200	RF, MEMS, SoC	0.9
2005+	$>$ 200	500	Mix of all into a Complex SoC	1.0

* Multi-Disciplinarity Index

VLSI Challenges : Key Technological Areas

- Top-down Digital System Design and its Optimization for Silicon Implementation.
- CISC / RISC / DSP / Parallel / Application Specific Instruction Set Processors (ASIP).
- Low-Power Circuit Design, Logic Design, Technological and Layout issues.
- Mixed Analog-Digital Design.

VLSI Challenges : Key Technological Areas

- Signal Integrity and other DSM issues.
- RF IC Design and associated issues.
- High-Speed / High-Resolution / Low-Power A/D and D/A Architectures and Design.
- Signal Processing (Digital and Analog) and ASSP.
- Design of Signal Conditioning and Interface Circuits for Sensors.

VLSI Challenges : Key Technological Areas

- Micro-system Design (MEMS/MEOS).
- Testing and Testability.
- Speech Recognition and Synthesis.
- Synthesis and Design Automation techniques for all the above design areas.

VLSI Challenges : Application Areas

- Telecommunications and Networking.
- High-end Computing.
- Multimedia and Visualization.
- Information Compression and Decompression.
- Man-machine Interface.
- Industrial Control and Robotics.

VLSI Challenges : Application Areas

- Automotives and Transportation.
- Energy Management and Power Conversion.
- Medical Electronics and Implantable Devices.
- Strategic Systems.
- Environment Control and Pollution Monitoring.
- Consumer Electronics and Home Appliances.

New VLSI Challenges

Inter-disciplinary knowledge integration and harnessing.

Wedding the knowledge of standards in the application areas with the VLSI-SoC architectural knowledge and the knowledge of key technical areas to realize competitive microelectronic solutions.

Academic Challenges in the Near Term

Indian Books on VLSI Subjects : Text Books and Specialized Reference Books.

Indian Academic VLSI CAD Tools : Physical, Circuit, Logic, RTL, HDL, Synthesis, Test, . . .

Indian Academic-R&D Processors : CISC/RISC/DSP Cores, Compilers, IP Blocks, . . .

Government's New Initiatives for VLSI Education

Efforts are underway in the DIT/MCIT, Government of India to start a new project for developing manpower in the area of VLSI Design and Embedded Systems.

The summary of today's discussions can provide a valuable input towards this effort.