

#### History:

Workshop Title	Venue	Date	Partici- pants
1st VDAT	Chennai	January 7, 1998	30
2 <sup>nd</sup> VDAT	New Delhi	August 6-7, 1998	70
3 <sup>rd</sup> VDAT	New Delhi	August 20-21, 1999	120
4 <sup>th</sup> VDAT	New Delhi	August 25-26, 2000	150
5 <sup>th</sup> VDAT	Bangalore	August 16-18, 2001	220
6 <sup>th</sup> VDAT	Bangalore	August 29-31, 2002	300
7 <sup>th</sup> VDAT	Bangalore	August 28-30, 2003	300

## **Topics of Workshops:**

The following workshops will be held concurrently:

Workshop on *High-level Design* will discuss issues related to system-level synthesis, embedded systems, codesign, core-based design of SoC, timing convergence, high-level synthesis, logic synthesis, memory synthesis, and FPGA synthesis. Workshop on *Physical Design and VLSI Technology* will discuss all issues related to physical design and process related aspects of integrated circuits, such as layout, fabrication, packaging, opto-electronic circuits, MEMS, deep submicron and nanometer devices.

Workshop on *Testing and Verification* will discuss issues related to testing, testability, and verification of digital designs, memories, analog designs, and mixed-signal designs, and circuits containing deep-submicron and nanometer devices. In addition, *VLSI Education Day* (*VED 2004*) will be held as part of VDAT 2004, on August 26, 2004.

#### Conference Committee

#### General Chair:

C.P. Ravikumar, Texas Instruments India **Technical Program Committee** Vishwani Agrawal, Rutgers University, USA Shabbir Batterywala, Synopsys, India Navakanta Bhat, IISc, Bangalore, India Bhargab Bhattacharya, ISI Calcutta, India Srimat Chakradhar, NEC, USA V. Hande, Infosys, India S. Karthik, Analog Devices, India Anshul Kumar, IIT Delhi, India S. Mahant-Shetti, KARMIC, India N.S. Murthy, Philips Semiconductors, India R. Parekhji, Texas Instruments, India C.P. Ravikumar, Texas Instruments, India Partha Ray, National Semiconductors, India J.N. Roy, SCL Chandigarh, India Vineet Sahula, MREC Jaipur G.H. Sarma, VLSI Society of India Narendra Shenoy, Synopsys, India Alok Singh, Virage Logic, India P. Sridhar, Controlnet, India S. Srinivasan, IIT Madras, India CR Venugopal, SJCE, Mysore

V. Visvanathan, Texas Instruments, India

## **CALL FOR PARTICIPATION**

8<sup>th</sup> IEEE VLSI Design & Test Workshops August 26-28, 2004

## Mysore, India

Sponsored by VLSI Society of India and Infosys
In Cooperation With: IEEE-CS-TTTC and
IEEE EDS/SSCS Bangalore Chapter
IEEE Mysore Chapter, SJCE Mysore
(Confirmation Awaited)
<a href="http://vlsi-india.net">http://vlsi-india.net</a>
Related Site: http://vlsi.nj.nec.com/

# Local Organization Chair

C.R. Venugopal, SJCE, Mysore, vdat04local@vlsi-india.net Fellowships Chair Narasimha Kaulgud, SJCE, Mysore vdat04fellow@vlsi-india.net Finance and Registration Chair Navakanta Bhat, IISc, Bangalore

### ADDRESS FOR CORRESPONDENCE

Authors should submit extended abstracts of **at least 4 pages** or full papers of **at most 10 pages**. Your submission should represent original contribution and should not have been submitted to other forums. It is important that abstracts bring out the contribution and novelty of the paper. Survey papers are not acceptable as submissions. However, proposals for embedded tutorials (1 hour or 2 hour duration), and proposals for panel discussions are invited. Send your submissions through the Docman system accessible from <a href="http://vlsi-india.net">http://vlsi-india.net</a> as well as <a href="http://vlsi.nj.nec.com/">http://vlsi-india.net</a> as well as <a href="http://vlsi.nj.nec.com/">http://vlsi.nj.nec.com/</a> For questions relating to technical program, submissions, and sponsorships, write to:

C.P. Ravikumar Texas Instruments, India Wind Tunnel Road, Murgeshpalya Bangalore 560017 Email: <u>ravikumar@vlsi-india.net</u>

FAX: 91-80-5269456

## **IMPORTANT DATES**

Last Date for submission: March 31, 2004 Notification of acceptance: May 15, 2004 Last day to receive final manuscript: June 1, 2004 Workshop Dates: August 26-28, 2004

The workshops are a forum to promote R&D in all aspects of VLSI in India. Authors of accepted papers will not be required to submit full papers, although they are encouraged to do so. All authors of accepted papers are, however, required to submit Presentation Foils of their talks in PowerPoint or PDF format. Final submissions (full papers or presentations) will be available as Workshop Proceedings. Papers presented in the workshops may be revised and published/presented in other forums.

