VLSI Design and Test Workshops 2004
August 26-28, 2004
Advance Program for Day 1
VLSI Education Day

Time	Description		
8.00 to 9.00 AM	Registration		
9.00 AM	Inauguration. Venue – Mahatma Gandhi Auditorium, Infosys Leadership Institute		
9.15 AM	Session D1-Keynote Talk by Prof. Dinesh Sharma of IIT Bombay. Venue: Mahatma Gandhi Auditorium, ILI		
10.15 AM	Tea Break		
11.00 AM	**Session D1-Tutorial Venue – Room Subhash Chandra Bose**		**Session D1-Education Venue – Room Bhagat Singh**
	Jagdish Rao, Texas Instruments, India. *VLSI Design Challenges to Enable SoC*. Tutorial.		**Shekhar Pradhan** and Felica W. Blanks, Bluefield State College, West Virginia, USA. *The Role of Institutional Development and Advancement Office in Promoting Undergraduate VLSI Education - A Role Model Concept*
			Vineet Sahula, MNIT Jaipur. *VLSI Curriculum in an Indian University.*
			Mini Panel Discussion – *Student Projects in VLSI: Is a Change in Perspective needed? Experts from the field of VLSI will debate on this topic.*
1.00 PM	Lunch and Time to Visit Exhibits. Exhibits will be located in Room Ashoka		
2.00 PM	Session D1-FNAQ		
	Frequently Not Asked Questions! Expert panelists will answer questions from the audience. Technical questions can be sent to ravikumar@vlsi-india.net		
3.30 PM	Tea and Time to Visit Exhibits		
4.00 PM	Session D1-Panel Venue – Mahatma Gandhi Auditorium		
	Taking VLSI Education to the Next Level of Competence. What is the need of the hour today – quantity or quality? Several M.Tech programs on VLSI and Embedded Systems have been started in the country and short-term training programs in these areas are being offered by training institutions. Do we now have the critical mass? Is the training being provided adequate? How can we take hi-tech education to the next level of competence? How can educational institutions, industry, and governmental organizations synergize towards this cause?Expert Panelists will debate on this topic. The names of the panelists will be announced.		
5:30 PM	**Session D1-Poster-1- FPGA Applications - Venue – Subhash Chandra Bose**	**Session D1-Poster-2 Logic Design Venue – Room Bhagat Singh**	**Session D1-Poster-3 Systems Design Venue – Room Chanakya**
6.30 PM	Break for Dinner		

Time	Description		
	Advance Program for Day 2 - August 27, 2004		
9.00 AM	**Session D2-Keynote1**		
	Keynote Speech - "Challenges in growing high-tech organizations in India - Infosys Perspective" by Mr **Kris Gopalakrishnan,** Infosys. **Venue – Mahatma Gandhi Auditorium.**		
10.00 AM	**Tea and Time to Visit Exhibits**		
10.30 AM	**Session D2-EDA Venue – Room Subhash Chandra Bose**	**Session D2-Analog Venue – Room Bhagat Singh**	**Session D2-Test Venue – Room Chanakya**
	Shabbir H. Batterywala, Synopsys (India) Pvt. Ltd., Narendra V Shenoy, Synopsys Inc., Richard Rudell and Nidhi Sawhney *Parallelizing a Statistical Capacitance Extractor*	**M. Shankaranarayana Bhat**, NITK Surathkal, Rekha S. and Jamadagni H S., IISc, Bangalore *Design of Current-mode CMOS Multiple- valued Latch*	**Sarath Kumar Reddy,** Ravi Dasari, Mentor Graphics India, Venkata Rangam, TI India. *An ATPG Approach for 2-D Array Configurable Logic Structures*
	Subhashis Mandal, Abhishek Somani, Shamik Sural and Amit Patra, IIT Kharagpur and Robert Drury, National Semiconductor, Santa Clara, USA. *A Connection Graph based Variable Wire Width Approach to Analog Routing*	G.Suresh, G.L.Biswas, **K.D.N.V.S.Prasad** and A.T.Kalghatgi. *Configurable I/Q Modulator using Cordic based DDS Architecture.*	Shantanu Gupta, **Santanu Chattopadhyay** and Tarang Vaish, IIT, Guwahati. *A Novel Approach to Reduce Test Power Consumption*
	Sreekanth K.M., Lionel Dahyot Vinod Kumar. Texas Instruments India Ltd. *Novel Approach to Solve IP Integration Problems in an Era of SOC.*	**M. Shankaranarayana Bha**t, NITK Surathkal and Jamadagni H S., IISc, Bangalore *Design of Current-mode Flash ADC*	Susanta Chakraborti, Pradyut Sarkar and Arindam Karmakar, University of Kalyani. *Fault Diagnosis by Spectral Method*
12.00 Noon	**Break**		
12.15 PM	**Session D2-Crosstalk Venue – Room Subhash Chandra Bose**	**Session D2-Circuits Venue – Room Bhagat Singh**	**Session D2- Validation Venue – Room Chanakya**
	A. Ravishankar and Aniket Singh, IIT Madras. *Maximization of Aggressor Influence in Crosstalk-Delay Testing*	**Anil V Nandi,** BVBCET, Hubli, Saumen Das and S.K.Lahiri, IIT, Khargpur. *Development of Silicon Piezoresistive Accelerometer for Avionics Applications+*	**N.Vijayaraghavan** and Dimple Lalwani, ST Microelectronics Ltd. *Automated Silicon Debugging Methodology for Validating Standard Cells.*
	Sachin Shrivastava and Sreeram Chandrashekhar, Texas Instruments, India. *Crosstalk Noise Analysis at Multiple Frequencies*	**Sunil Kumar Vashishtha,** Intel India Tech Pvt Ltd, Bangalore and Basbi Bhaumik, IIT Delhi. *Design of 1.5V, 10-bit, 1200 mV Input range, CMOS, Pipelined Analog-to-Digital Converter.*	**Subhashis Mandal,** Siddhartha Mukhopadhyay, Amit Patra and Santosh Biswas, Advanced VLSI Design Lab , IIT Kharagpur. *A Formal Approach to On-Line Monitoring of Digital VLSI Circuits.*
	Sushrant Monga, Paras Garg and Frederic Hasbani. ST Microelectronics. *A Mathematical analysis of analog and digital summation tecniques in compensation block for I/O buffers .*	**Venkatesh C**. and Navakanta Bhat, IISc, Bangalore. *A MEMS Oscillator based on displacement sensing principle.*	**Subash Chandra Bose**, CEERI, Vishal Gupta and Dinesh Jain BITS, Pilani. *Fault Observability Analysis of CMOS Op-amp in Frequency domain.*
1.00 PM	**Lunch and Time to Visit Exhibits**		
2.00 PM	**Session D2-Keynote2**		
	Ralf Pferdmenges, Infineon Technolgogies. *Design Methodology for sub-0.1 um Technologies.*		
2.45 PM	**Session D2-Memory Venue – Room Subhash Chandra Bose**	**Session D2-Embedded Venue – Room Bhagat Singh**	**Session D2-Verification-1 Venue – Room Chanakya**
	Sreedhar Natarajan, Emerging Memory Technologies, USA. *Emerging Non Volatile Memory: Technological Promise Or Industrial Hoax.*	**Atanendu Sekhar Mandal**, CEERI. *Designing an Embedded Processor : Specifications to Implementations.*	**Sunil Kakkar**, Freescale Semiconductors. *Advanced Processor Architectures- The Verification Challenge.*

3.45 PM	Tea and Time to Visit Exhibits		
4.15 PM	**Session D2-Logic Venue – Room Subhash Chandra Bose**	**Session D2-Technology Venue – Room Bhagat Singh**	**Session D2-Verification-2 Venue – Room Chanakya**
	P Vijayakumar and K Gunavathi, PSG College of Technology. *Performance Optimization Of CMOS Circuits Using Retiming Algorithm With Stepwise Charging*	**Anuj Madan**, Punjab Engg College, Chandigarh, Sumeet Jindal, B.Prasad and P.J.George. *An Efficient Monte Carlo Device Simulator to calculate Velocity Ovesrhoot in MOSFETs.*	**Pritam Roy,** Pallab Dasgupta and P P Chakrabarti, IIT Kharagpur. *An Assertion-based Language for Generating Test Sequences for Complex Temporal Behavior.*
	S. Sarkar, Rajeevan Chandel and R.P. Agarwal, IIT, Roorkee. *Voltage-Scaled Repeaters for Low- Power Long Interconnections in VLSI Circuits.*	**Harish B.P.,** Srinivasan R., and Navakanta Bhat, IISc Bangalore. *Process Sensitivity Evaluation of 90nm CMOS Tecnology With Gate-to-Source/Drain Overlap Length as a Device Design Parameter.*	**K. Uday Bhaskar**, G. Chandramouli, and V. Kamakoti, IIT Madras. *Parikhsa - A functional Verification Architecture for x86 Processors.*
	Subhendu Kumar Sahoo, BITS, Pilani and Chandra Shekhar CERI. *A Compact Fast Parallel Multiplier Using Modified Equivalent Binary Conversion Algorithm.*	**Suresh Nalluri**, IISc Bangalore, A.P.Shiva Prasad. *Response Surface Methodology Based Design Approach for Yield Enhancement of Analog Integrated Circuits.*	
	Sridhar Krishnamurthy, SASTRA, Deemed University. *Implementation of Advanced Encryption Standard (AES) algorithm in a resource limited FPGA.*		**Bhaskar Pal**, A. Banerjee, P. Dasgupta, P.P. Chakrabarti, IIT Kharagpur and K. Chaitanya, Mentor Graphics, Hyderabad. *A Simulation Coverage Metric for Analyzing the Behavioral Coverage of an Assertion Based Verification IP.*
	Hande V, Uday Prabhu, Shardul Bapat, Infosys Technologies Ltd., India. *Real Time Interface between Automotive ECUs and a Simulator.*		
6.00 PM	**Session D2-Poster1 Applications Venue – Room Subhash Chandra Bose**	**Session D2-Poster2 Analog Circuits Venue – Room Bhagat Singh**	**Session D2-Poster3 Test & Verification Venue – Room Chanakya**
7.00 PM	Break for Dinner		

Time	Description		
	Advance Program for Day 3 - August 28, 2004		
9.00 AM	**Session D3-Keynote 1**		
	Keynote by Dr Sunil Sherlekar of Tata Consultancy Services		
10.00 AM	**Tea and Time to Visit Exhibits**		
10.30 AM	**Session D3-FPGA Room – Subhash Chandra Bose**	**Session D3-Technology 1 Room – Bhagat Singh**	**Session D3-Test-1 Room - Chanakya**
	Shaila Subbaraman, Walchand College of Engg. *FPGA/CPLD Based Solution to Stretch the Speed of Microprocessor / Microcontroller Based Instrumentation.*	**Kanishka Biswas**, S. Das, K. Dey, D. K. Maurya and S. Kal, Microelectronics Centre, IIT Kharagpur. *Study of Single Crystalline Silicon (100) Surface Topography Etched in KOH Solution.*	
	B. Venkataramani, G. Lakshminarayanan, M. Yousuff Shariff, T. Rajavelu and M. Ramesh, National Institute of Technology,Tiruchirappalli. *Self tuning circuit for FPGA based wave pipelined multipliers.*	**Vinod Kumar**, IIT Kharagpur. *Wet Etching and Patterning of BST Film for MEMS Infrared Detector.*	**Debesh Kumar Das**, Jadavpur University and Bhargab Bhattacharya, ISI Calcutta. *Redundancy and Undetectability of Faults in Logic Circuits: A Tutorial.*
	Gaurav Singh Nim and B S Chauhan, IRDE.*FPGA Implementation of Multiple Target Segregator.*	**Sudeb Dasgupta** and Ritambhar Roy, Indian School of Mines, Dhanbad. *Charactersiation of Gate Oxide Leakage Current of NANO-MOSFET Using Green's Function.*	
11.30 AM	**Break**		
11.45 AM	**Session D3-DSP-1 Room – Subhash Chandra Bose**	**Session D3-Technology-2 Room – Bhagat Singh**	**Session D3-Test-2 Room – Chanakya**
	G Thavasi Raja, S. Rajaram and V. Abhai Kumar, Thiagarajar College of Engineering, Madurai. *An FPGA Implementation of Code Phase Shift Keying Baseband Decoder.*	**Rajesh Kumar Sangati**, Sowjanya Syamala and Navakanta Bhat, IISc Bangalore. *Capacitance Sensing Techniques for MEMS Gyroscope.*	**Vishal Dalal**, SASKEN Communication Technologies Ltd., Bangalore. *Single Full Chip Vector for Functional Testing.*
	Prashant Ramrao Deshmukh, Dr P D Polytechnic, Amravati. *FPGA Implementation of Subband Image Encoder using*	**Srinivasan R** and Navakanta Bhat, IISc, Bangalore. *Reassessment of Channel Engineering in Sub-100nm MOSFETs.*	**Sarveswara Tammalli** and Jais Abraham, Texas Instruments (India) Ltd. *Hierarchichal ATPG Static Pattern Compression.*
	Arun Chokkalingam, PSNA College of Engg. *Implementation of Convolutional Encoder and Viterbi Decoder*	**Ganesan S Iyer** and Rajendra M. Patrikar, Visweswariya National Institute of Technology, Nagpur. *Effect on Surface Roughness on Physical Design Parameters.*	**D. Sharma,** L. Kamath, A. Gupta, IIT Mumbai. *Dynamic Error Cancellation in Fast Sigma Delta ADC.* **Invited Talk.**
12.45 PM	**Lunch and Time to Visit Exhibits**		
1.30 PM	**Session D3-Logic Room – Subhash Chandra Bose**	**Session D4-DSP-2 Room – Bhagat Singh**	**Session D4-Power Room – Chanakya**
	Chandra Mohan Umapathy, *Celstream Technologies Pvt Ltd. High Speed Squarers.*		**Syed Saif Abrar,** Philips. *Early, Fast & Accurate Software Power Estimation for Embedded Digital Signal Processors.*
	T.S.B.Sudarshan and Ganesh T.S. BITS, Pilani. *Hardware Architecture for Message Padding in Cryptographic Hash Primitives.*	**Soujanna Sarkar** and Subash Chandar Govindarajan, Texas Instruments, India. *Embedded Tutorial : DSP Architectures.*	**Lakshmi Prabha Viswanathan**, Government College of Technology Coimbatore and Elwin Chandra Monie, TPGIT Vellore. *Power Estimation in Embedded Systems From a Pre-characterized Module Library.*

	Ganesan S Iyer and Rajendra M. Patrikar, Visweswariya National Institute of Technology, Bajaj Nagar. *An Application of Neural Network Learning to Physical Design Optimization in VDSM Technology.*		**Lakshmi Prabha Viswanathan**, Government College of Technology Coimbatore and Elwin Chandra Monie, TPGIT Vellore. *Dynamic Power Management in an Embedded System for Multiple Service Requests.*
	Dipankar Das, Rajeev Kumar and Partha P. Chakrabarti. IIT Kharagpur. *Code Compression using Unused Encoding Space for Variable Length Instruction Encodings.*	**Vaishali B Mungurwadi** and A.S.Dhar, BVBCET, Hubli. VLSI Implementation of Viterbi Decoder.	**Siddharth Tata**, Siddharth Garg and Ravishankar Arunachalam, Indian Institute of Technology, Chennai. *Gate Level Dynamic Power Estimation in the Presence of Varying Process Parameters.*
	V. Appandai Raj, **D. Jovin Vasanth Kumar**, R. Madhu Karthikeyan, S. Rajaram, V. Abhai Kumar, TCE, Madurai. *FPGA Implementation of OFDM Transceiver.*	**Mallikarjunaswamy Shivagangadharaiah Muttad,** Bapuji institute of Engineering & Technology, Davangere. Ashok Rao, IISc, Bangalore and D.V. Poornaiah, IIT, Bangalore. *Systolic Array based VLSI Architecture for Motion Estimation in Video Compression Applications.*	**Satya Sridhar Narayanabhatla,** Kiran Satyamangala Jaisimha**,** Wipro Technologies, India and Binoj Xavier, Magma Design Automation, India. *nWATT: Power Planning Methodology In Physical Design.*
	Prashant Ramrao Deshmukh, DR P D Polytechnic, Amravati. *FPGA Implementation of DWT Based Image Compression Coder.*		
3.00 PM	**Tea and Time to Visit Exhibits**		
3.30 PM	**Session D3-Panel**		
	A panel discussion will be held to discuss a topic of relevance to Indian VLSI industry. The topic and the		
5.00 PM	**Workshop Conclusion**		

Conference Committee

General Chair: C.P. Ravikumar, Texas Instruments India (ravikumar@vlsi-india.net)

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Registration Information:
Registration permits you to participate in all the technical sessions and tutorials organized as part of the workshops. Refreshments and lunch will be provided to all registrants at no extra charge. Please send your registration fee through a draft made out to "*VLSI Design and Test Workshops, 2004*". **Make the draft payable at Bangalore.** The draft must be sent to **Sunil Patil, Finance Chair, VDAT 2004, Texas Instruments India, Bagmane Tech Park, Opposite LRDE, C.V. Raman Nagar Post, Bangalore 560093.** If you wish to register *on the spot*, drafts and cash payment in Indian rupees are acceptable. We will not be able to accept Foreign Currency or Credit Card payments. The current exchange rate is approximately 1 US dollar = 45 Indian rupees. Even those of you who are thinking of registering on the spot are requested to communicate your desire to attend VDAT 2004 to vdat04regn@vlsi-india.net Since the conference venue is the campus of a private company, we need to work with the Security personnel of Infosys to make the process of entering the campus and registering a smooth one. Your cooperation in this regard is appreciated.

Registration Fees Before July 20, 2004

	Indian Participant	Foreign Participant
Academic Institution	Rs. 2000	USD. 50
Non-academic Institution	Rs. 5000	USD. 150

Registration Fees After July 20, 2004

	Indian Participant	Foreign Participant
Academic Institution	Rs. 2500	USD. 75
Non-academic Institution	Rs. 6000	USD. 175

Venue Information:

- The venue of VDAT 2004 is the **Infosys Leadership Institute** (ILI) located at Hootagalli, Mysore. This is located in the Hebbal Electronics City, about 20 km from the Mysore Railway Station or Bus Station. The drive takes about 45 minutes – please factor this in your plan. The facility is right opposite the L&T Infotech. The approximate fare by auto-rickshaw from Railway station or Bus station is about Rs 100/- (US $3.00).
- A map of the Mysore city is available from http://www.mapsofindia.com/maps/karnataka/mysore.htm
- Information about hotels close to the Workshop venue is given at: http://www.vlsi-india.net/events/vdat2004/venue.shtml - This site is continually updated with more up-to-date information; please visit the site. If you need help in booking a room, please contact the local organization committee at vdat04orgn@vlsi-india.net
- Directions to ILI campus:
    1. **Approach #1:** Approach from KRS Road, keep going until you find Royal Inn, where you make a left. You should see VDAT 2004 banners - follow the directions to reach the venue.

2. **Approach #2:** When you reach Mysore city Toll gate, proceed to KR Circle and then to Hunasur Road. Go past Premier Studio. Make a right at Yashaswini marriage hall. You will see Kaines Hotel and VDAT 2004 banners - follow the directions to reach ILI campus.

Accomodation:

Hotels	Tarriff	Distance from Bustand	Distance from Infosys
Sagar Residency #64/1, Ashoka Road, Mysore-570 001 Ph: (0821) 2441049, 2434399	Single room – Rs. 380 Double room – Rs. 480	½ Km	6 to 7 Kms.
Hotel Chakravarthy (opp.Head Post Office), Ashoka Road, Mysore-570 001 Ph: (0821) 2446199, 2449526.	Double room – Rs. 225	½ Km	6 to 7 Kms.
Hotel Guptha #252/B, Ashoka Road, Mysore-570 001 Ph: (0821) 2449002, 2443073, 2445089.	Single room – Rs. 250 Double room – Rs. 290, Rs. 390	½ Km	6 to 7 Kms.
Nandini Lodge Next to Bustand, Irwin Road, Mysore. Ph: (0821) 2447085, 2447155, 5260422	Single room – Rs.175 Double room – Rs. 250,350	Next to Bustand	7 to 8 Kms.
Hotel Maruthi Palace #2927 Bangalore-Nilgiri Road, Mysore Ph: (0821) 2429586, 2442452	Single room – Rs. 250-Rs. 800. Double room – Rs. 385	Close to Bustand	7 to 8 Kms.
Ganesh Palace Inn L-17 , Chandraguptha Road, Mysore-1 Ph: (0821) 2428985, 5266020	Single room – Rs. 200,350 Double room – Rs. 400, 450	Close to Bustand	7 to 8 Kms.
Hotel Sanjeevi Palace, Bangalore- Nilgiri Road, Lashkar Mohalla Mysore-1 Ph: (0821) 5555020, 2436645	Single room – Rs. 250 Double room – Rs.300	Close to Bustand	7 to 8 Kms

Weather Information: The weather in Mysore during August is pleasant (temperatures ranging in 25 to 30 degrees centigrade), with some chances of shower.

Tour: If there is sufficient interest, a 1-day tour of Mysore city will be organized on Sunday, August 29th, for the participants. Please write to vdat04orgn@vlsi-india.net and confirm your participation if you are interested.

Related Event: International Conference on VLSI Design, Kolkata, 2005: http://vlsi.ccrl.nj.nec.com/

For updated information, please visit us at www.vlsi-india.net