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12th IEEE VLSI Design and Test Symposium

July 23-26, 2008

Venue: Learning Centre, Wipro Campus, Electronics City, Bangalore, India

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Advance Program for July 23, 2008 (Wednesday) - Day-1			
08.30 AM - 9.30 AM	Registration and Breakfast		
09.30 AM - 11.00 AM	**Session 1A: Tutorial – I** **RF Design and Test** **Venue:** Room-Coral **RFIC Design and Testing for Wireless Communications** ***Vishwani Agrawal*** *and* ***Foster Dai,*** *(Auburn University)*	**Session 1B: Tutorial – II-A** **Low-power** **Venue:** Room-Mermaid **SoC Power Management Architecture Design and Verification** ***Bhanu Kapoor****, Mimasic;* ***Shankar Hemmady****, Synopsys; and* ***Sandeep Aggarwal****, TI India*	**Session 1C: Tutorial – III** **Design Verification Methodologies** **Venue:** Room-Oyster **Holistic Verification: Myth or The Magic Bullet?** ***Pradip Thaker****, Analog Devices*
11.00 AM - 11.30 AM	Tea Break		
11.30 AM - 01.00 PM	**Tutorial Continues**	**Tutorial Continues**	**III – B Foundations of Design Verification- Formal and Functional Approaches** ***Ansuman Banerjee; Kausik Datta;*** *and* ***Amit Roy*** *(Interra Systems India Pvt. Ltd.)*
01.00 PM - 02.00 PM	Lunch		
02.00 PM - 03.00 PM	**Tutorial Continues**	**Tutorial Continues**	**Tutorial Continues**
03.00 PM - 03.30 PM	Tea Break		
03.30 PM - 05.30 PM	**Tutorial Continues**	**Session 1B-A: Tutorial – II-B** **Ultra Low-Power Processors for Embedded Systems** ***Atul Lele*** *(Texas Instruments) and* ***Gurjit Singh Gill*** *(Gill Instruments)*	**III – C Static Rule Checking and Cross-domain crossing** ***Kaushik De,*** *Synopsys*
End of Day-1			

Tutorial – I: RF Design and Test

RFIC Design and Testing for Wireless Communications
Vishwani Agrawal and Foster Dai (Auburn University)

Tutorial – II: Low-power Design

Part-1 (4 hrs) **SoC Power Management Architecture Design and Verification**
Bhanu Kapoor, Mimasic; **Shankar Hemmady**, Synopsys; and **Sandeep Aggarwal**, TI India

Part-2 (2 hrs) **Ultra Low-Power Processors for Embedded Systems**
Atul Lele (Texas Instruments) and **Gurjit Singh Gill** (Gill Instruments)

Tutorial – III: Design Verification Methodologies

Part-1 (1.5 hrs) **Holistic Verification: Myth or The Magic Bullet?**
Pradip Thaker, Analog Devices

Part-2 (3 hrs) **Foundations of Design Verification- Formal and Functional Approaches**
Ansuman Banerjee; **Kausik Datta**; and **Amit Roy** (Interra Systems India Pvt. Ltd.)

Part-3 (1.5 hrs) **Static Rule Checking and Cross-domain crossing**
Kaushik De, Synopsys

The speakers are expert practicing professionals in the respective areas. More details of the tutorial and biographies of the speakers are available from the VDAT website – http://vlsi-india.org/events/vdat2008/tutorials.shtml

Information

Please watch updates on VDAT at http://vlsi-india.org/ The idea behind the VLSI Design And Test (VDAT) Symposium is to promote Research and Development on all aspects of VLSI in India. This symposium is a forum for free discussion of hot and emerging topics in VLSI. It provides a meeting place for VLSI professionals working in India and abroad. We have been holding this event since 1998, and the participation in the event has steadily gone up every year. The VLSI Industry in India and academic community working in the area of VLSI has provided immense support to the symposium.

VDAT is sponsored by the ***VLSI Society of India****. Please consult http://vlsi-india.org/vsi/ for more information on VSI''s mission and goals. If you are unable to view the page, please send a mail to vdat@vlsi-india.org for a softcopy of the application form.*

Consult http://vlsi-india.org/vsi/activities/index.shtml for updates on the activities of the VLSI Society of India. If you wish to become a member of the VLSI Society of India, you can download the form from http://vlsi-india.org/vsi/membership/index.shtml (form is included at the end of this document).

Tutorial – I: RF Design and Test

RFIC Design and Testing for Wireless Communications

Speakers: Vishwani Agrawal and Foster Dai, (Auburn University)

The boom of wireless and mobile networks has led to an ever-increasing demand for high performance, low power, and low cost RFIC design. Advances in silicon and silicon-germanium based technologies can now provide highly integrated system-on-chip (SOC). With WLAN and cellular standards operating in very different frequency bands, market leading wireless solutions have to offer multi-mode interoperability with transparent worldwide usage. The increasing demand for wireless multimedia applications such as video streaming keeps pushing future wireless systems to support higher data rates at higher link reliability and over greater distances. A multiple-input multiple-output (MIMO) wireless system in combination with space-time signal processing allows increased data rate, improved transmission range and link reliability without additional costs in bandwidth or power.In spite of a significant motivation, the engineering education today lacks coverage of RFIC design and test techniques. Wireless networks provide plenty of design challenges with both academic and commercial values. This course provides information about fundamentals of wireless communication systems and building block designs of wireless transceivers.

The course starts with a discussion on multi-com radios for multi-standard coexistence issues on RFIC designs. It then focuses on wireless transceiver IC designs such as low-noise-amplifier (LNA), mixer, and voltage-controlled oscillator (VCO) designs. The course also presents advanced topics on RFIC testing for wireless transceivers.This one-day tutorial can best be best described as introductory. It is suitable for engineers who did not have any experience with RFICs, those who work on IC design and wish to sharpen their understanding of modern methods, and engineering managers.

Tutorial – II: Low-power Design

Part-1 (4 hrs) **SoC Power Management Architecture Design and Verification**

Speakers: **Dr. Bhanu Kapoor** (Mimasic), **Shankar Hemmady** (Synopsys), and **Sandeep Aggarwal** (TI India)

We are at the crossroads of some fundamental changes that are taking place in the semiconductor industry. Power consumption has become one of the most important differentiating factors for semiconductor products due to a major shift in the market towards handheld consumer devices. Power is a primary design criterion for bulk of the semiconductor designs now. Power is a key reason behind the shift towards multi-core designs as increase in power consumption limits increases in clock speed at the rate we have seen in the past.

Voltage is the strongest handle for managing chip power consumption. Dynamic power is proportional to the square of supply voltage and leakage power has a linear relationship with it. In addition, leakage power has an exponential relationship with the threshold voltage of the device. This implies that if voltage can be controlled to optimally meet the performance then there can be much to be gained in terms of power savings.

This tutorial focuses on introducing fundamentals of the SoC power management design and verification to the attendees. We look in detail at some of key power management techniques that leverage voltage as a handle: Power Gating (PG), Power Gating with Retention (RPG), Multiple Supply Voltages (MSV), Dynamic Voltage Scaling (DVS), Adaptive Voltage Scaling (AVS), Multi-Threshold CMOS (MTCMOS), and Active Body Bias (ABB).

The use of above mentioned techniques imply certain power management architecture design and partitioning of design in terms of voltage islands that are controlled through power management signals. We look at the challenges in power management architecture design utilizing some examples that incorporate state-of-the-art power management techniques. The use of above mentioned techniques also imply new challenges in validation of designs as new power states are created. We look into the characteristics of typical power states that exist in such designs and detail the techniques used in design validation. Techniques that leverage simulation, formal, and rule-based techniques are described in detail using examples. We make use of industrial design examples to aid explanation of these points.

Part-2 (2 hrs) **Ultra Low-Power Processors for Embedded Systems**

Speakers: Atul Lele (Texas Instruments) and **Gurjit Singh Gill** (Gill Instruments)

Providing electrical power to operate an embedded system can be a challenge, since the system may be a portable or an implanted device and has to rely on batteries or harvested energy. With the growth of mobile Internet devices, which support a rich set of media applications, conserving mission-mode power requires careful consideration so as to avoid frequent recharging of batteries. In implanted devices, it may be virtually impossible to change or recharge batteries. As examples, consider a camera that can be implanted into the eye of a blind/partially blind person, or a wireless sensor network node that can be implanted in a locket that is placed on a wild animal for tracking its movements. Architectural breakthroughs are required to reduce the power dissipation of the processor to Pico watts and still be able to provide adequate processing speed. In this tutorial, we will discuss the principles of operation of an ultra low-power processor, which is popularly used in several embedded applications. We will also provide an overview of several emerging applications such as biomedical engineering where such processors are used.

Tutorial – III: Verification

Part-1 (1.5 hrs) **Holistic Verification: Myth or The Magic Bullet?**

Pradip Thaker, Analog Devices

With advances in submicron technologies over last decade, multi-million gate ICs have become a cliché. With growth in size of the design, the diversity in functionality on a single-chip has proportionally grown while the time-to-market pressures have remained unchanged. On a single-die, it is common to have variety of combinations of newly developed digital as well as mixed-signal/analog circuits, integration of in-house and/or 3rd party IPs, integration of mega-blocks such as RAMs and ROMs, single or multiple instances of processor core(s), implementation of newly developed algorithms or standards with strict requirement for logical and electrical compliance, variety of standard and non-standard interfaces, integration of building blocks created through orthogonal design flows such as RTL and custom design. With convergence of these multiple disciplines on a single-die, verification of such IC is beyond the scope of any single verification approach. Even brute-force cumulative deployment of all verification techniques each of which is traditionally used to tackle a respective challenge is insufficient to produce high-quality robust first silicon. In this presentation, a holistic verification strategy will be defined and discussed with aim to provide guidelines for high-confidence verification sign-off of high-end multi-million gate devices with feature and flow diversities. Trade-offs of various emerging and incumbent verification techniques will be presented along with best practices from both, academics and industry.

Part-2 (3 hrs) **Foundations of Design Verification- Formal and Functional Approaches**

Ansuman Banerjee; **Kausik Datta**; and **Amit Roy** (Interra Systems India Pvt. Ltd.)

Design verification is the process of ensuring that a design meets its specifications. This tutorial introduces the concept of hardware design verification, and briefly covers the different methods of design verification and their respective strengths and weaknesses. On one hand, in this discussion, we intend to provide an in-depth understanding of formal verification with discussion on symbolic and SAT-based approaches along with a comprehensive overview of the basic building blocks of a formal verification tool. On the other hand, we discuss in detail the established principle of simulation-based functional validation along with state-of-the art developments in this area. In the concluding part of the discussion, we mention two advanced issues of interest in the verification community today. The tutorial will also involve brief demos of some verification tools available in the public domain.

Part-3 (1.5 hrs) **Static Rule Checking and Cross-domain crossing**

Kaushik De, Synopsys

As design complexities are growing, design verification problem is exploding. Simulation remains the main vehicle for design verification. However, design complexities make it extremely difficult to cover all cases of the design. Formal verification are used to prove properties of the design, however the capacity of the tool remains an obstacle. In addition, Formal verification technology usage requires deep expertise. Static Checker technology offers another very good alternative, which can identify potential issues in the design by doing static analysis of the design. For example, it can identify if the design can have simulation synthesis mismatch or potential race condition during simulation, or operand type or width mismatch, unintentional latch in the design, etc. In addition, it can detect many fundamental issues such as clock/reset/connectivity, etc. It can also detect correctness in signal connectivity in multi-power domain designs. Hence, deployment of static checker technology will greatly enhance the design verification capability.

The modern designs have many clock domains, and special care need to be taken in designing the part where signal traverses from one clock domain to another. Designing and verifying interaction between signals between asynchronous clock domains is major challenge, because signals crossing clock domains need to follow strict rules to ensure correct functionality. Many design re-spin happens due to bug in clock-domain crossing issues. In order to verify correctness of clock-domain crossing, comprehensive methodology needs to be followed encompassing structural, formal and simulation techniques.

Advance Program for July 24, 2008 (Thursday) - Day-2

VLSI Education Day

08.00 AM - 09.00 AM	**Registration and Breakfast**	
09.00 AM - 09.30 AM	**Inauguration**	
09.30 AM - 10.30 AM	**Session 2A-1: Keynote Talk** **Teaching and Research in Microelctronics at IIT Bombay- A view from Lake Powai** **Speaker:** ***A.N.Chandorkar,*** *IIT Bombay* **Chair:** TBA **Venue:** Room-Coral	
10.30 AM - 11.00 AM	Tea Break	
11.00 AM - 01.00 PM	**Session 2A-2: Invited Talk** **Venue:** Room-Coral **Analog and Mixed Signal Design – Need for a Curriculum Upgrade** ***K.Radhakrishna Rao****, TI India* Analog circuits are an integral part of a signal chain, since the environmental attributes that we wish to measure or control, such as ambient temperature, atmospheric pressure, relative humidity, etc., are analog in nature. This talk will look at what upgrades are needed in today's curriculum to prepare the graduating engineer to the challenging task of designing, verifying, integrating, and testing analog circuits that are part of a system-on-chip.	**Session 2A-3:** **Venue:** Room-Mermaid **Discussion** **Creating more Ph.D. holders in Cutting Edge Technologies** **Moderator: *Dipankar Nagchoudhuri****, DA-IICT, Gujrat* **Panelists: *Dinesh Sharma*** *(IITB);* ***G.S.Visweswaran*** *(IIT Delhi);* ***Sham Banerji*** *(Texas Instruments India); and* ***Debashis Dutta****, Senior Director, Industrial Promotion - Electronics & Hardware Manufacturing Division* There is agreement that India needs more Ph.D. holders in cutting edge technologies such as system-on-chip integration, embedded systems, nanotechnology, biomedical applications, etc. Ph.D. holders are needed in the academia to teach effectively and create and sustain research programs. Ph.D. holders are needed in industry and government research labs to spec and define new products and to make the interaction between academia and industry more effective. In this discussion panel, we will invite some of the leaders from the three sectors to make a position statement about the projected need for Ph.D. holders and on what is being done to achieve this goal. An informal brainstorming session or mailing list will be announced where others can air their views.
01.00 PM - 02.00 PM	Lunch	
02.00 PM - 03.30 PM	**Session 2A-4: Panel Discussion** **Venue:** Room-Coral **Growing the Right Talent for a Growing Semiconductor Industry** **Moderator: *C.P. Ravikumar*** *(Texas Instruments)* **Panelists: *Jaswinder Ahuja*** *(India Semiconductor Association/Cadence),* ***S. Karthik*** *(Analog Devices India),* ***Manav Subodh*** *(Intel India),* ***N.S. Murty*** *(NXP Semiconductors),* ***A. Vasudevan*** *(Wipro)* The semiconductor industry in India has come a long way in the past 20 years. Design companies have moved up from library cell design and characterization to full system-on-chip designs. CAD companies have moved from a predominantly "service-provider" mode to software product and IP development. Several start-up companies have also sprung up and some have achieved a degree of success. Some companies have also ventured into development of embedded systems. Sourcing the right talent for the growing semiconductor industry, retaining this talent, and growing the talent have been challenges the industry has faced for several reasons: • Confusing array of undergraduate and postgraduate programs (*Electrical*, *Electronics*, *Communications*, *IT*, *Computer* and permutations) with major overlaps in content • Unstructured campus placement (rush to get talent young, confusion between "IT" and semiconductor, improper talent matching • Lowered entry bar for educational institutions in USA/Europe • Exalted expectations in compensation • Unrealistic expectations in work • Lack of "soft skills" • Lacking eco-system for growth The panelists will examine these issues and hint at how they have attempted to solve some of the problems in their own ways. While some of these problems can be attacked independently, collective community effort is needed to address the others - the panel will initiate a debate in this direction.	

03.30 PM –04.00 PM	Tea Break		
04.00 PM - 04.45 PM	**Session 2A-5: Research Scholar Forum** **Venue:** Room-Coral **Chair:** ***C.P. Ravikumar*** *(Texas Instruments)* Research Scholars will be invited to present a brief overview on their Ph.D. theses. Experts will be invited to attend the session and provide feedback.		
04.45 PM - 05.00 PM	Break		
05.00 PM - 06.00 PM	**Session 2A-6** **RF Design** **Chair:** ***C.P. Ravikumar*** *Texas Instruments India* **Venue:** Room-Coral	**Session 2B-6** **Digital Design** **Chair:** ***C.R.Venugopal****, SJCE* **Venue:** Room-Mermaid	**Session 2C-6** **Biomedical Applications** **Chair:** ***Mahant S. Shetti****, KarMic* **Venue:** Room-Oyster
	A Pulse Width modulated DC-DC Buck Converter using On-chip Inductor *Rohan Kesireddy;Jyothi Bhaskarr Amarnadh; Genemala Haobijam; and* ***Roy Paily***** (IIT Guwahati)* 91 Poster Paper	**Novel Circuits for Two's Complement of a Binary Number** ***Rahul Badghare*****; Raghavendra Deshmukh (VLSI Design Labs, VNIT, Nagpur); and Rajendra Patrikar (CRL, India)* 71 Poster Paper	**Sensor Integration in an RFID Tag for Monitoring Biomedical Signals** *Sandeep Reddy Munnangi;* ***Roy Paily*****; Rakesh Singh Kshetrimaym; Genemala Haobijam; and Manikumar Kothamasu (IIT Guwahati)* 144 Poster Paper
	Design of an RF CMOS LNA using 0.25 micron Technology ***Pranjal Rastogi*** *(Texas Instruments); Karthik Jayaraman (Analog/ RF Research group, Oregon State University, USA); and Rajnish Sharma* (BITS, PILANI)* 27 Poster Paper	**High-Speed, High-Throughput Pipelined and Parallel Architecture for SPIHT algorithm** ***Anilkumar Nandi***** (BVB College of Engg. & Tech)* 146 Poster Paper	
End of Day-2			

Advance Program for July 25, 2008 (Friday) - Day-3			
08.00 AM - 09.30 AM	**Registration and Breakfast**		
09.30 AM - 10.30 AM	**Session 3A-1: Keynote Talk** **Venue:** Room-Coral **Enabling Systems on a Chip to Test Themselves** ***Jacob A. Abraham**, The University of Texas at Austin* **Chair:** ***Shabbir Batterywala**, Synopsys*		
10.30 AM - 11.00 AM	Tea Break		
11.00 AM – 12.00 PM	**Session 3A-2** **Analog-1** **Chair:** ***Dinesh Sharma**, IIT Bombay* **Venue:** Room-Coral	**Session 3B-2: Invited Talk** **Biomedical Applications** **Chair:** ***Shyam Vasudev**, Philips Software* **Venue:** Room-Mermaid	**Session 3C-2** **Testing-1** **Chair:** ***Jacob A. Abraham**, The University of Texas at Austin* **Venue:** Room-Oyster
	High Speed CML Transmitter with on-chip PVT compensation for improved Gain and Linearity errors ***Navin Kumar***; Umesh Shukla; and Sankarareddy Kommareddi (IBM India Pvt Ltd)* 42 Regular Paper	**Connected Healthcare** **Dinesh Bhatia** University of Texas at Dallas	**Adapting Scan Compression to Designs** ***Rohit Kapur***; Anshuman Chandra; Yasunari Kanzawa; and Tom Williams (Synopsys Inc.,)* 17 Embedded Tutorial
	Ultra Wideband Variable Gain Amplifier Design for Software Defined Radio Applications *Neeraj Kumar; Parul Chopra; and **Roy Paily*** (IIT Guwahati)* 113 Regular Paper		**Containing Switching Activity in Scan Compression** ***Pramod Notiyath***; Tammy Fernandes; Ashok Anbalan; Santosh Kulkarni; Rajesh Uppuluri; Jyothirmoy Saikia; Glenn Boyer; Rohit Kapur; and Tom Williams (Synopsys Inc.,)* 162 Short Paper
12.00 PM - 01.00 PM	**Session 3A-3: Invited Talk** **Moving Event Localization using Multihop Cellular Sensor Networks** ***Uday B. Desai**, IIT Bombay* **Chair:** ***Dinesh Sharma**, IIT Bombay*		**Session 3C-3: Invited Talk** **Venue:** Room- Dolphin **Low Power Verification - Overcoming the Challenges** ***Srikanth Jadcherla**, Synopsys Inc.* **System Verilog for VLSI Design - Prospects and Challenges** ***N.S.Murty**, NXP Semiconductors* **Chair:** ***Subir Roy**, TI India*
01.00 PM - 02.00 PM	Lunch		
02.00 PM - 03.00 PM	**Session 3B-3: Keynote Talk** **Venue:** Room-Coral ***Electronic Design Evolution in India and Its Impact on Semiconductor Design*** ***Sudip Nandy**, Wipro Technologies* **Chair:** ***Shabbir Batterywala**, Synopsys*		
03.00 PM - 04.00 PM	**Session 3A-4** **Analog-2** **Chair:** ***G.S.Visweswaran**, IIT Delhi* **Venue:** Room-Coral	**Session 3B-4** **Digital Design-1** **Chair:** ***N.S.Murty**, NXP Semiconductors* **Venue:** Room-Mermaid	**Session 3C-4** **Testing-2** **Chair:** ***Sudhakar Reddy,** University of Iowa; and **Virender Singh*** **Venue:** Room-Oyster
	A CMOS Comparator Circuit Optimized for Power-Delay Product and Input-Output Isolation *Amit Kumar Gupta (Cadence Design Systems, Noida); and **Chetan Parikh*** (DA-IICT Gandhinagar)* 10 Regular Paper	**High Performance Elliptic Curve Crypto-processor for FPGA Platforms** *Chester Rebeiro; and **Debdeep Mukhopadhyay*** (Dept of CSE, IIT Madras)* 51 Regular Paper	**Test Pattern Reduction by Simultaneously Pulsing Interaction Clocks** ***Xijiang Lin*** (Mentor Graphics Corp); Sudhakar Reddy (University of Iowa); and Irith Pomeranz (Purdue University)* 18 Regular Paper
		Mesh-of-Tree Based Network-on-Chip Architecture Using Virtual Channel Based Router ***Santanu Kundu***; and Santanu Chattopadhyay (IIT Kharagpur)* 49 Regular Paper	**On-chip Test Circuits for Fast Interconnects** ***Rajkumar Satkuri***; Marshnil Dave; M. Shojaei Baghini; and Dinesh Sharma (IIT, Bombay)* 32 Regular Paper
	Performance Comparison of CNFET and CMOS Based Full Adders at The 32nm Technology Node ***Tarun Agrawal***; Anurag Sawhney; Abdul Kadir Kureshi; and Mohd. Hasan (Aligarh Muslim University)* 93 Regular Paper		**A Primal-Dual Solution to Minimal Test Generation Problem** ***Vishwani Agrawal***; and Mohammad Shukoor (Auburn University)* 150 Regular Paper
04.00 PM - 04.15 PM	Tea Break		

	Session 3A-5 **Analog-3** **Chair:** ***A.N.Chandorkar,*** *IIT Bombay* **Venue:** Room-Coral	**Session 3B-5** **Digital Design-2** **Chair:** ***C.P. Ravikumar*** *Texas Instruments India* **Venue:** Room-Mermaid	**Session 3C-5** **Testing-3** **Chair:** ***Vishwani Agrawal****, Auburn University* **Venue:** Room-Oyster
04.15 PM - 05.15 PM	**Slew Rate Improvement Technique for High Frequency and Large Amplitude Signals** ***Benny Thomas****; and Roy Paily (IIT Guwahati)* 133 Short Paper	**Low Latency LSB First Bit-Parallel Systolic Multiplier over GF(2m)** ***Hafizur Rahaman****; Prasenjit Ray; and Somsubhra Talapatra (BESUS)* 134 Short Paper	**Cellular Automata and LFSR Coupling for Pattern Generation: A Feasibility Study** *Susmit Maity; Pushan Mitra; Prasenjit Ghosh; and* ***Biplab Sikdar**** *(Bengal Engg. And Science Univ.)* 41 Regular Paper
	Selecting an Optimum Bias Current for An Auxiliary Amplifier in Gain Boosting Amplifier for Power Optimization ***Vinayak Pachkawade**** *(VNIT, Nagpur); and Rajendra Patrikar (CRL, India)* 130 Short Paper	**Design, Simulation and Testing of a High Performance 15-4 Compressor** ***Shubhajit Roy Chowdhury****; Aniruddha Roy; Aritra Banerjee; and Hiranmay Saha (Jadavpur University)* 61 Short Paper	
	Design of Low Power Low Pass Filter for ECG Application With Deep Submicron Technology ***Amey M. Walke****; Waman S. Khokle (VNIT, Nagpur); and Rajendra Patrikar (CRL, India)* 117 Short Paper		
05.15 PM - 05.30 PM	Break		
	Session 3A-6 **Timing** **Chair:** ***C.P. Ravikumar*** *Texas Instruments India* **Venue:** Room-Coral	**Session 3B-6** **Digital Design-3** **Chair:** **Venue:** Room-Mermaid	**Session 3C-6** **Interconnect** **Chair:** ***Rajeevan Chandel,*** *NIT Hamirpur* **Venue:** Room-Oyster
05.30 PM - 07.00 PM	**Analysis And Comparison of Delay Elements and a New Delay Element Design** ***Sujan Manohar****; and Pavan Torvi (Texas Instruments)* 46 Regular Paper	**Optimization of High-Performance RF MEMS Capacitive Shunt Switch for Phase- Shifter Applications at Ku band** ***Avra Kundu**** *(Jadavpur University); Sasanko Maji (Indian Association for the Cultivation of Sciences); Bhaskar Gupta; Samir Lahiri; and Hiranmay Saha (Jadavpur University)* 86 Poster Paper	**Cross-talk Mitigation in Coupled VLSI Interconnects** *Gargi Khanna; Preeti Sharma;* ***Rajeevan Chandel**** *(NIT Hamirpur HP); Sankar Sarkar (FET, Mody Institute of Tech. & Sci., Rajasthan)* 37 Embedded Tutorial
	Dynamic Profiling in Virtual Prototype Environment ***Praveen Kumar**** *(NXP Semiconductors India Pvt L)* 67 Poster Paper		**A Fast and Efficient Crosstalk Closure Methodology for Multi-million Gate SOCs** ***Chirag Gupta****; Soujanna Sarkar (Texas Instuments India); and Saravanan Karunavel (Montalvo Systems)* 38 Regular Paper
	HCFG Based Approach for Evaluation of SMP Model for System-on-Chip Communication ***Ulhas Deshmukh****; and Vineet Sahula (Malaviya National Inst. of Tech. Jaipur)* 164 Poster Paper		**A Framework for Dynamic Analysis of SoC Power Grids at Planning Stage** ***Jairam Sukumar**** *(Texas Instruments India); and Jayesh Jayarajan (Delhi College of Engineering)* 1 Poster Paper
			Bus Synchroniser technique used in Dynamic frequency Scaling ***Shalini Sharma**** *(Freescale)* 35 Poster Paper
07.15 PM - 08.45 PM	**Banquet Dinner**		
End of Day-3			

Advance Program for July 26, 2008 (Saturday) - Day-4

08.30 AM - 09.30 AM	Registration and Breakfast		
09.30 AM - 10.30 AM	**Session 4A-1** **Keynote Talk** **Physical Design EDA Challenges for 32nm and Beyond** ***Mysore Sriram**, Intel* **Chair: *Shabbir Batterywala,** Synopsys* **Venue:** Room-Coral		
10.30 AM - 01.00 PM	**Session 4A-2** **Analog-4** **Chair: *Sambuddha Bhattacharya,** Synopsys* **Venue:** Room-Coral	**Session 4B-2** **Technology-1** **Chair: *Shabbir Batterywala,** Synopsys* **Venue:** Room-Mermaid	**Session 4C-2** **Low power-1** **Chair: *Vishwani Agrawal**, Auburn University* **Venue:** Room-Oyster
	Macromodel based Fault simulation of Opamp using Parameters Estimation ***Kiran Kumar Garje***; Srikanth Pam; Amitava Banerjee; Santosh Biswas; and Siddhartha Mukhopadhyay (IIT Kharagpur)* 161 Regular Paper	**Metal Gate CMOS from the Device Variability Perspective** ***H. C. Srinivasaiah*** (EPCET); Navakant Bhat (Indian Institute of Science)* 15 Regular Paper	**Dynamic Threshold PMOS Switch for Power Gating** ***Naushad Alam***; Abdul Kadir Kureshi; and Mohd. Hasan (Aligarh Muslim University)* 36 Regular Paper
			A History based Technique for Low Power Bus Encoding ***Santanu Chattopadhyay***; and Srujan Reddy (IIT Kharagpur)* 19 Short Paper
		Analytical Modeling and Simulation of Fixed-Fixed beam RF MEMS Resonator ***Vaishali Mungurwadi*** (BVB College of Engg. & Tech.,); Uday Wali (KLE College Belgaum)* 142 Regular Paper	**Input Assignment Technique for low Power Circuit Testing** ***Subhadip Kundu***; Kanchan Manna (IIT KGP); Tapas Kr. Maiti (College of Engg. & Management, Kolaghat); and Santanu Chattopadhyay (IIT Kharagpur)* 75 Short Paper
		Presentation **Design Methodology for a 2.5GHz Native Quad Core x86 Processor** ***Prasad Kuppa**, AMD*	**Presentation** ***Jayantha Lahiri**, ARM Embedded Technologies*
01.00 PM - 02.30 PM	Lunch		
02.30 PM - 04.00 PM	**Session 4A-4** **Memory-1** **Chair: *Preeti Ranjan Panda**, IIT Delhi* **Venue:** Room-Coral	**Session 4B-4** **Verification** **Chair: *Subir Roy,** Texas Instruments India* **Venue:** Room-Mermaid	**Session 4C-4** **Low power-2** **Chair: *C.P. Ravikumar** Texas Instruments India* **Venue:** Room-Oyster
	Efficient Modeling of Memory Controllers in SystemC ***Aravinda Thimmapuram***; and Raghunath Gannamaraju (NXP Semiconductors)* 83 Embedded Tutorial	**Efficient ECO implementation using Logical Equivalence Checking** ***Sarveswara Tammali***; Mayank Jindal; and Shailesh Ghotgalkar (Texas Instruments)* 124 Embedded Tutorial	**Power Estimation of Different Arbitration Techniques for On-Chip Bus Based Reconfigurable Soc Platform** ***Srinviasan N***; HemaChitra S; and Vanathi P.T. (PSG College of Technology)* 47 Short Paper
	600 MHz 18 Kb Ternary Content Addressable Memory ***M Sultan M Siddiqui***; and G S Visweswaran (IIT Delhi)* 110 Regular Paper	**Case Studies Towards a Platform Independent Framework for Formal Verification of Hybrid Systems** *Kusum Lata (CEDT, IISc Bangalore); **Jairam Sukumar*** (Texas Instruments); Subir Roy (SDTC, TI India); H.S.Jamadagni (CEDT, IISc Bangalore)* 64 Regular Paper	**Low Power Discrete time FIR Pulse Shaping Filter Design Algorithm using Linear Programming Technique** ***Shalini Sharma*** (Freescale)* 59 Poster Paper
	March Test for Linked Faults in Random Access Memories ***Sanjay Thakur*** (Texas Instruments)* 82 Regular Paper		**Leakage-aware Synthesis of Multilevel Logic Circuits based on BDD Manipulation and Output Phase Selection** ***Saurabh Chaudhury*** (NIT Silchar); and Santanu Chattopadhyay (IIT Kharagpur)* 54 Poster Paper
	A SEU Tolerant Distributed CLB RAM for In-Circuit Reconfiguration *Karthik Kumar Srivatsa; Shyam Venkatesh; N. Rama Subramaniam (IIT Madras); Shoaib Mohammad (NIT Trichy); Noor Mahammad; and **Veezhinathan Kamakoti*** (IIT Madras)* 55 Short Paper	**Functional Verification of Sleep Mode Operation in Low Power Designs at RTL** *Rudra Mukherjee; **Amit Srivastava***; Gargi Mukherji; and Abhishek Kesh (Mentor Graphics)* 90 Regular Paper	**Performance Comparison of CNFET And CMOS based 8T SRAM Cell in Deep Submicron** *Abdul Kadir Kureshi; **Naushad Alam***; and Mohd. Hasan (Aligarh Muslim University)* 28 Poster Paper

End of Symposium

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Treasurer, VLSI Society of India
Finance Chair (VDAT 2008)
Texas Instruments (India) Pvt Ltd
Bagmane Tech Park, Opp. LRDE
C.V.Raman Nagar, Bangalore – 560 093
vsiaccount@vlsi-india.org

Registration Information:

- Registration permits you to participate in all the Technical sessions and Tutorials organized as part of the Symposium, and includes refreshments and lunch on all days.
- Please send your registration fee through a draft made out to "***VDAT Symposium 2008***", payable at Bangalore**.**
- The draft must be sent to *Mr.Gopal Naidu, Finance Chair (VDAT 2008), Texas Instruments India, Bagmane Tech Park, C.V. Raman Nagar, Bangalore 560093.*
- If you wish to register *on the spot*, drafts and cash payment in Indian rupees are acceptable. We will not be able to accept Foreign Currency or Credit Card payments.
- The current exchange rate is approximately 1 US dollar = 39 Indian rupees.
- Even those of you who plat to register on the spot are requested to communicate your desire to attend VDAT 2008 to vdat-regn@vlsi.india.org with a copy to vdat@vlsi.india.org with details of vehicle registration number (if any) and laptop number (if any). Without this, you may face difficulties during registration.
- If you are registering for a tutorial, indicate the first and second preference of the tutorial. There are limited seats in each tutorial. If we cannot register you in the tutorial of your choice, we will refund the amount.
- A processing fee of Rs 500/- will be applied against all cancellations.

Symposium Registration Amount

	Fellow	Indian Faculty/ Student	Indian Industry VSI/ IEEE Member	All Foreign Participants	Others
Before June 30, 2008	Rs.1500/=	Rs.2500/=	Rs.6000/=	US$ 150.00	Rs.7000/=
After June 30, 2008	N/A	Rs.3000/=	Rs.7000/=	US$ 200.00	Rs.8000/=

Tutorial Registration Amount

Before June 30, 2008	Rs.1000/=	Rs.1500/=	Rs.2000/=	US$ 100.00	Rs.2500/=
After June 30, 2008	Rs.1500/=	Rs.2000/=	Rs.2500/=	US$ 125.00	Rs.3000/=

Since the conference venue is on the Campus of a private organization, we need to work with the Security personnel of the organization to make the process of registration a smooth one. Your cooperation in this regard is appreciated.

- ✓ Registration for participants
  - Mandatory Govt ID card
  - Registration Entry from Gate 7
  - Registered participants, to provide contact number, and Institute/ Company address

Please send a mail to vdat-local@vlsi-india.org and inform your vehicle's registration number and Laptop number if you will come in your private vehicle and/or bring your laptop.

History of VDAT:

Event Title	Venue	Date	Participants
1st VDAT	Chennai	January 7, 1998	30
2nd VDAT	New Delhi	August 6-7, 1998	70
3rd VDAT	New Delhi	August 20-21, 1999	120
4th VDAT	New Delhi	August 25-26, 2000	150
5th VDAT	Bangalore	August 16-18, 2001	220
6th VDAT	Bangalore	August 29-31, 2002	300
7th VDAT	Bangalore	August 28-30, 2003	300
8th VDAT	Mysore	August 26-28, 2004	250
9th VDAT	Bangalore	August 10-13, 2005	350
10th VDAT	Goa	August 9-12, 2006	250
11th VDAT	Kolkata	August 8-11, 2007	250

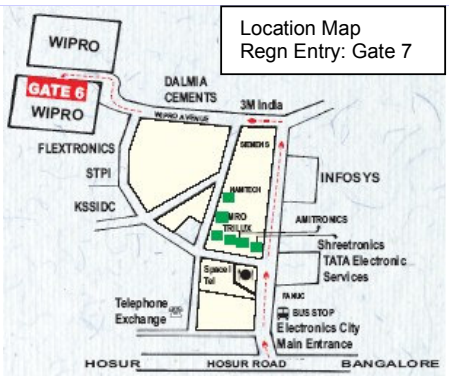
Venue Information:

The venue of the Symposium is the Learning center on the Wipro campus, located in Electronics City. Each of the rooms has a capacity of 100. All Rooms have video hooking for the plenary events. Speakers will have facilities such as DLP projector, cordless microphone, and whiteboard.

Since the conference venue is on Wipro Campus, we need to work with the Security personnel of the organization to make the process of registration a smooth one. Your cooperation in this regard is appreciated.

There are several hotels in Bangalore and information on these is available from the Internet. We plan to provide bus pickup/drop service from the following two areas: (a) Indian Institute of Science (b) Majestic. Details will be announced on the website. If you plan to use your own transport, please note: to reach Electronics city, you must travel on Hosur road and enter the Phase I gate. See the location map shown here. The distance to the venue from Railway station is ~20 km and from the Airport, about 15 km**.** Due to traffic during morning rush hour and evening rush hour, the actual transit time may be significantly high. *Please plan your travel.*

Weather in Bangalore during August is pleasant, bordering on chilly, with occasional showers.



12th IEEE VLSI Design and Test Symposium

July 23-26, 2008
Venue: Learning Center, Wipro Campus, Electronics City, Bangalore, India
Website: vlsi-india.org

Sponsored by
VLSI Society of India
http://vlsi-india.org/vsi/

REGISTRATION FORM

Name of the participant: (Please use block letters.)

Category: (Tick appropriate)	Fellow	☐	VDAT 2008 Fellowship No:
	Faculty / Student: VSI/ IEEE member	☐	VSI/ IEEE Membership No:
	Indian Industry: VSI/ IEEE member	☐	VSI/ IEEE Membership No:
	Author	☐	Paper No/s:
	Foreign Participant	☐	
Address for Correspondence:	**Designation:** Student ☐ Faculty ☐ Industry ☐ Other ☐ **College/ Company Name:** **Permanent address:**		

E-mail: (Compulsory):

Choice of tutorial: **T1** ☐ **T2** ☐ **T3** ☐
T1: RF Design and Test; **T2**: Low-power Design; **T3:** Design Verification

Telephone:

Details of DD enclosed	Tutorial:		DD Number:	
	Symposium:		Dated:	
	Total Amount:		Bank:	

Attend: (tick appropriate)
T1 ☐ T2 ☐ T3 ☐ Symposium ☐
Symposium + T1 ☐ Symposium + T2 ☐ Symposium + T3 ☐

Signature

Tutorial Registration Amount		
T1, T2 or T3 July 23, 2008	*Before June 30, 2008*	*After June 30, 2008*
Fellow	Rs 1000	Rs 1500
Faculty/ Student	Rs 1500	Rs 2000
Indian Industry VSI/ IEEE Member	Rs 2000	Rs 2500
Foreign Participant	USD 100	USD 125
Others	Rs 2500	Rs 3000

Symposium Registration Amount		
July 24-26, 2008	*Before June 30, 2008*	*After June 30, 2008*
Fellow	Rs 1500	N/A
Faculty/ Student	Rs 2500	Rs 3000
Indian Industry VSI/ IEEE Member	Rs 6000	Rs 7000
Foreign Participant	USD. 150	USD 200
Others	Rs 7000	Rs 8000

Mail the completed registration form and DD to the following address:

Mr. Gopal Naidu
Treasurer, VLSI Society of India
Finance Department
Texas Instruments (India) Pvt Ltd
Bagmane Tech Park
C.V. Raman Nagar, Bangalore 560093
Phone: 080-2509 9363; **FAX**: 2509 9717
vsiaccounts@vlsi-india.org

- *The DD to be made out to "**VDAT Symposium 2008**" payable at **Bangalore, India**. On the rear side of DD, please write **Towards VDAT2008** and/or **T1/T2/T3** as applicable.*
- *The DD and form to be sent to the VDAT2008 Finance Chair, to Bangalore address mentioned on the left.*
- *You must also enter the above details electronically at our website to receive information from us regularly*
- *If an author is also a fellow recipient, please tick both.*
- *Queries regarding registration must be sent only to: vdat-regn@vlsi-india.org with a copy to vsiaccounts@vlsi-india.org*

Note:	Symposium registration fee includes registration material, lunch and refreshments on all the days. If registering separately for Symposium and Tutorial, please submit separate forms for each. Transport and stay arrangements are the responsibility of the participants.

Please watch the VDAT website or follow the vdat@yahoogroups.com mailing list for any updates to the program. Since the space for tutorials is limited, we may be forced to shortlist participants. If we are unable to register you, you will be intimated by e-mail, and a refund will be made by the VLSI Society of India.

VSI Membership Form

For New membership and renewals

VLSI Society of India

http://vlsi-india.org/vsi/

Registered Society under KSR Act 1960, Rule 1961

E-mail: **vsiaccounts@vlsi-india.org**, **vsisecy@vlsi-india.org**

New Members to affix photograph.

1. Existing Membership No: ☐☐☐☐ (Quote additional Old No. If any): ☐☐☐☐

Member (tick as applicable): ☐ **Student** / ☐ **Non-student** / ☐ **Corporate**

2. Your Name:

3. Your Profession/ Designation:

4. Your e-mail address:

5. Your Contact address:

6. Your Professional address (if different from above):

7. Your Area of specialization:

8. Would you like to review papers in events organized by VSI? :

9. How many papers are you willing to review? :

10. Your Brief bio-data: Attach separately

11. How can you contribute to the activities of VSI? :

12. What Activities would you like VSI to organize? :

13. Details of Payment:

Cash:	
DD no:	
Dated:	
Drawn on Bank:	
Amount:	

I agree to be a member of the VLSI Society of India and have read and understood the charter of the society. I will actively contribute towards the objectives of the society.

Place and Date: **Member Signature**

Category	**Membership Rates:**		**Mail the form along with the DD to:**
	Yearly	**5-yearly**	**Mr. S.R. Gopal Naidu**, Treasurer VSI
Student Member:	Rs. 500/=	N/A	Texas Instruments India Pvt. Ltd
Non-student member:	Rs. 1,000/=	Rs 4,500/-	Bagmane Tech Park, Adjacent to LRDE, C.V. Raman Nagar
Corporate member:	Rs. 10,000/=	Rs 45,000/-	Bangalore: 560 093 **(FAX: 91-80-25048213)**

The DD to be made out to: "VLSI Society of India" and payable at Bangalore.

- *Please also enter the details in the online membership form http://vlsi-india.org/vsi/activities/reg.shtml to update records.*
- *Processing the card subject to the DD receipt. Please allow two weeks.*
- *The photograph is for official records only and will not be imaged onto the membership card.*
- *Inscribe **"Towards VSI Membership - New/ Renewal"** at the rear side of DD. Students to attach college credentials.*
- *The same form to be used for a new membership or Renewal. In the event of change of address, please update online.*
- *Please do not send scanned images of DD or the Form. Processing the card subject to the DD receipt. Allow two weeks.*
- *Become a VDAT Yahoogroup member to receive updates on all announcements. Details on http://vlsi-india.org/docs/mailgroup.shtml*

Recommended by VSI Members:

1.	**Name**	**Membership No.**	**2.**	**Name**	**Membership No.**
Signature			**Signature**		