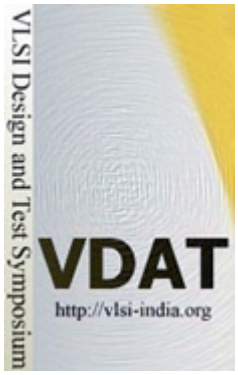


To promote applications and research related to all aspects of VLSI in India

Organized by

http://vlsi-india.org/vsi/

13th IEEE / VSI VLSI Design and Test Symposium

July 8-10, 2009

Venue: Wipro Campus

Wipro EC Phase 4 (EC4), Gate 10, Tower 20

Electronic City, Hosur Road, Bangalore, India

IEEE Bangalore Section

IEEE-CAS Bangalore Chapter

In Co-operation with

IEEE-CS TTTC

PES Institutions, Bangalore

RV Col of Engg Bangalore

IISc. Bangalore

Corporate Sponsors

Cranes Software Intl Ltd

Wipro Technologies

Texas Instruments India

ARM Embedded Technologies

Final Program for July 8, 2009 (Wednesday)

08.30 AM - 9.30 AM	Registration and Breakfast			
09.30 AM - 11.00 AM	**Venue** Cranes Software Intl Ltd Bangalore **1A-1: Tutorial - T1** **Open Source Embedded System Development using Beagleboard** ***Syed Khasim*** *(Texas Instruments India)*	**Venue** Wipro Campus, Electronic City, Phase 4, Gate 10, Tower20, Bangalore **Rooms: Flint:** Ground Floor**; Quest:** 2nd Floor; **Nova:** 1st Floor **1A-2: Tutorial - T2** **Room - Flint** **Compact Modeling and PDK's** ***Madabusi Govindarajan****,* *Tamilmani Ethirajan, Abhisek Dixit, and Josef Watts (IBM)*	**1A-3: Tutorial - T3** **Room - Quest** **Part I** **Test Cost Reduction Techniques: Current Practices, Challenges and Impact** ***Sarveswara Tammali**** *(Texas Instruments India)*	**1A-4: Tutorial - T4** **Room - Nova** **Part I** **Telemedicine** ***Poornima Mohanachandran,*** *i2i Technologies*
11.00 AM - 11.30 AM	Tea Break			
11.30 AM - 01.00 PM	T1 Continues	T2 Continues	T3-I Continues	T4-I Continues
01.00 PM - 02.00 PM	Lunch			
02.00 PM - 03.00 PM	Hands-on On Beagleboard	T2 Continues	**Part II** **Test Power Reduction Techniques: Current Practices, Challenges and Impact** ***C.P. Ravikumar*** *and* ***V.R. Devanathan*** *(Texas Instruments India)*	**Part II** **Assistive Devices for the Visually Impaired** ***M Balakrishnan**** *(IIT Delhi)*
03.00 PM - 03.30 PM	Tea Break			
03.30 PM - 05.30 PM	T1 Continues	T2 Continues	T3-II Continues	T4-II Continues
End of Day-1				

The speakers are expert practicing professionals in the respective areas. More details of the tutorial and biographies of the speakers are available from the VDAT website - http://vlsi-india.org/events/vdat2009/index.html

Information

Please watch updates on VDAT at http://vlsi-india.org/ The idea behind the VLSI Design And Test (VDAT) Symposium is ***to promote Research and Development on all aspects of VLSI in India****. This symposium is a forum for free discussion of hot and emerging topics in VLSI. It provides a meeting place for VLSI professionals working in India and abroad. We have been holding this event since 1998, and the participation in the event has steadily gone up every year. The VLSI Industry in India and academic community working in the area of VLSI has provided immense support to the symposium.*

VDAT is sponsored by the ***VLSI Society of India****. Please consult http://vlsi-india.org/vsi/ for more information on goals, activities of the VLSI Society of India. If you wish to become a member of the VLSI Society of India, you can download the form from http://vlsi-india.org/vsi/membership/index.shtml (form is included at the end of this document).*

For a larger image of the route map: http://vlsi-india.org/events/vdat2009/route-map.jpg

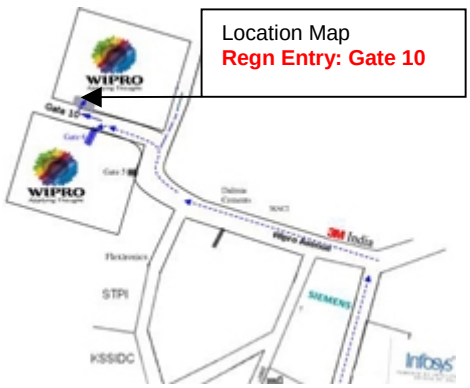
Venue Information:

The venue of the Symposium is the Learning center on the Wipro campus, located in Electronic City. To reach the campus, please travel on Hosur road and enter the Electronic City through Phase I gate.

Participants will have to go through Wipro's Security before entering the campus. Please carry a Government-issued photo-id such as passport or Driver's license. Please wear the security badge when you are in the campus and return it to the security personnel before leaving the campus.

There are several hotels in Bangalore and information on these is available from the Internet. See the location map shown here. The distance to the venue from Railway station is ~20 km and from the Bangalore International Airport, about 50 km**.** Due to traffic during morning rush hour and evening rush hour, the actual transit time may be significantly high. *Please plan your travel*. Weather in Bangalore during August is pleasant, bordering on chilly, with occasional showers.

Speakers will have facilities such as DLP projector, cordless microphone, and whiteboard.



Tutorial – T1 (Participants restricted to 20)

(**Venue:** Cranes Software Intl Ltd, # 5, Airport Road, Domlur Layout, Bangalore – 560 071)

Open Source Embedded System Development using Beagleboard

Syed Khasim *(Texas Instruments India)*

With the availability of low-cost platforms, open-source development of embedded systems is becoming possible for individual hobby-professionals and start-ups. In this tutorial, we will introduce the participants to the exciting world of open-source development using the Beagleboard as an example. Beagleboard is intended for low-power, high-performance embedded systems development and supports Linux operating system. A growing world-wide community of Beagleboard users collaborate on solving problems and come up with innovative solutions. In this tutorial, we will cover the following topics and provide some hands-on training on the Beagleboard.

The topics we will cover include:

- Introduction to Open Platforms
- Quick overview of the Beagle Board
- Open Software development tools
- Collaboration tools
- Validating beagle board peripherals with Linux tools on Beagle Board
- Introduction to Open Embedded
- Programming the DSP and ARM cores made easy
- Hands-on Training

Syed Mohammed Khasim started his career back in 2001 with Linux devices for Single board computers and TI DSP applications & solutions. In 2004 he joined Texas Instruments as a Linux Consultant through Wipro technologies. After spending last three years (2004 - 07) in TI head quarters (Dallas, Texas USA) as a Linux Consultant and Open Source Facilitator for Wireless software development & strategies, he moved back to India and joined as a Technical Lead for Open Platforms in DSPS / Catalog applications division of TI. In last couple of years, Khasim has pioneered and lead various initiatives in TI to meet the increase in demand for Mobile Linux on TI chipsets and processors. Khasim earned a bachelor's degree in Computer Science & Engg in 2001 from BMS college of Engineering, Bangalore, India.

Tutorials T2, T3 & T4 (**Venue:** Learning Centre, Wipro Campus, Electronic City, Hosur Road, Bangalore)

Tutorial – T2

Compact Modeling and PDK's

Madabusi Govindarajan, ***Tamilmani Ethirajan***, ***Abhisek Dixit,*** *and* ***Josef Watts*** *(IBM)*

This tutorial covers compact models and their roles and dependencies in a Process Design Kit (PDK). The emphasis throughout will be to understand the circuit consequences of compact models from an intuitive standpoint. We begin by dissecting a PDK and delve into the mutual dependencies of device views, modelcards, layout-versus-schematic (LVS) decks, and parasitic extraction (PEX) decks. We then pick up a "simple" device such as a poly resistor and demonstrate how harmonics and self-heating pose modeling challenges for RF front-end designs. Thereafter we escalate the device and model complexity to cover a variety of active and passive device models, culminating in PSP models for ultra deep submicron FET's. The roles of as-fit and centered models are analyzed in detail. Special emphasis is placed on FET A.C/Noise models and extraction, including the important role of the layout parametric cell-PEX boundary. Statistical modeling is also covered in detail, including Monte Carlo, fixed/functional corners, and statistical timing analysis.

Madabusi Govindarajan received his Bachelor's degree in Electrical Engineering from IIT-Madras in 1988, and the Ph.D degree also in Electrical Engineering from the University of Southern California, Los Angeles, in 1994. At USC he worked on high-speed circuits based on GaAs and InP HBT technologies. From 1994-99 he was a faculty member at the Department of Electrical Engineering, IIT-Bombay, where he became an Associate Professor. At IIT-B Govindarajan taught courses in analog circuits and electromagnetism, and pursued research projects in high-speed systems. From 1999-2002 he worked in the San Francisco Bay Area at LuxN, an innovative start-up in the metropolitan optical networking area. From 2002-05 he was with Scintera, a fabless Bay Area start-up that developed a path-breaking line of 10 Gbps electronic dispersion compensation IC's in standard CMOS. From 2005-2007 Govindarajan was with Signalguru, a Bangalore-based consultancy in high-speed test & measurement. In 2007 he joined IBM's Semiconductor R&D Center (SRDC) in Bangalore, where he is with the design enablement group, focusing on compact modeling of RF derivative processes. Govindarajan's technical interests are in high-speed/RF devices and circuits.

Tutorial – T3

Part-I: Test Cost Reduction Techniques, Current Practices, Challenges and Impact

Sarveswara Tammali* *(Texas Instruments India)*

Test cost is becoming increasingly significant percentage of COB (Cost of Build) in current SoCs (System-on-a-Chip), accentuated by the need of more testing required in shrinking technology nodes. This is even critical in low cost markets like consumer devices. Test quality, which is measured in defective parts per million (DPPM) is becoming aggressive in growing competitive market. So, it is often delicate trade-off that is required to plan test cost strategy given test quality requirements and vice-versa. Strategy includes DFT architecture, target ATE and multi-site configuration and test flow strategy. There are well known DFT techniques namely parallel test, scan compression, built-in-self-test (BIST), which are key techniques in the low cost strategy. Current practices of multi-site test, concurrent tests, scan compression and BIST are discussed. Challenges and impact of these techniques are discussed in detail in this tutorial. The tutorial also talks about some miscellaneous test cost reduction techniques that involve reduction of IDDQ stops and scan pattern optimization. Another important strategy for test cost reduction approach is to use low cost ATE (Automated Test Equipment) as a target tester for SoC. Some of common limitations of low cost ATE are frequency of interaction with DUT, accuracy of stimuli application and output strobe and limited number of tester resources. DFT and test pin muxing, timing closure needs to comprehend limitations of low cost ATE right from design start to be able to successfully utilize low cost ATE for most of tests if not all of manufacturing tests. Key challenges for product engineering team from multi-site point of view are power supply grouping, site-to-site variation, power supply noise and external components on board. In the last section, test cost reduction strategy is discussed which includes test time estimation and identifying critical test modes where test time reduction helps to reduce overall test cost are discussed.

Sarveswara Tammali, IEEE member, obtained an M.Tech in *VLSI Design Tools and Technology* from IIT Delhi (2001) and joined Texas Instruments India, where he has been responsible for DFT architecture, implementation and support for ramp for several multi-million System-on-a-Chip designs. He has presented several papers in both internal and external international conferences on topics related to Scan Compression, Test Cost Reduction and Failure Analysis. Currently he is actively involved in Test Cost Reduction process. He is also DFT lead for the SOC that has achieved lowest test cost (% of COB) at Texas Instruments and has won best RTP'ed device award with lowest test cost. He has earned his bachelor's degree in ECE from JNTU College of Engineering, Anantapur, Andhra Pradesh.

Tutorial – T3

Part-II: Test Power Reduction Techniques: Current Practices, Challenges and Impact

C.P. Ravikumar *and* ***V.R. Devanathan*** (*Texas Instruments India)*

In this part of the tutorial, the speakers will focus on test power reduction. Test power is important from the viewpoint of preventing packaging decisions, device reliability and test effectiveness. The speakers will cover some of the recent techniques for test power reduction, such as hierarchical techniques for power reduction, glitch power reduction, and low-voltage scan shift technique.

C.P. Ravikumar is a senior technologist at TI India. He is also the secretary of the VLSI Society of India since 2003. More details about him can be found at http://cpravikumar.tripod.com/

V.R. Devanathan obtained his B.E. from GCT, Coimbatore, M.Tech. (Computer Science) from IIT Madras, and Ph.D. (Computer Science) from IIT Madras. He has more than six years of industry experience. He is presently with Texas Instruments working on Design for Test related problems for the past five years. He has published papers in the area of Low-Power Testing in leading IEEE conferences and journals. His Ph.D. thesis won the *best thesis* award at the IEEE VLSI Test Symposium, 2008.

Tutorial – T4

Part-I: Telemedicine

Poornima Mohanachandran *(i2i Technologies)*

This tutorial will begin by addressing the question of how the medical profession can benefit from technology, in particular, VLSI technology. The tutorial will provide a perspective on the new developments in the area of Tele-Medicine. The tutorial will bring out research & development opportunities and challenges for Indian academia and industry. As an illustration, the topic of medical image compression will be considered and a demonstration will be given of the software developed by an Indian R&D house.

Poornima Mohanachandran has held many executive level management responsibilities at Texas Instruments. She was GM of product development for high performance data converters at Texas Instruments and most recently Director of Business Development for Medical Business at TI. Here she was working with TI customers and medical industry on new opportunities for semiconductor devices in Medical Applications. She has 20 years of industry experience covering all aspects of product development and business development. Presently she is with i2iTeleSolutions a company focused on telemedicine solutions. At i2i she is responsible for strategy and development of telemedicine solutions.

Part-II: Assistive Devices for the Visually Impaired

M Balakrishnan** (IIT Delhi)*

In the last three years, an inter-disciplinary group working in the area of embedded systems has been formed at IIT Delhi. The focus of the group has primarily been to design innovative devices for assisting visually impaired persons. In this period we have now worked on four projects that are listed below.

1. Smart Cane
2. Bus identification system
3. Braille tutor
4. Disha: Indoor navigation system

The projects have reached various stages of completion including prototyping and have resulted in one technology transfer done to a company and the second ready for technology transfer. The tutorial would focus on two aspects:

- Technical details and achievements of the four projects and
- A successful model for involving undergraduate students in embedded systems design activity

The tutorial would be accompanied by demonstration of prototypes of these projects. Visit for details - http://embedded.cse.iitd.ac.in/assistech

M Balakrishnan is a professor in the Computer Science Department, IIT Delhi. His research areas include Embedded Systems, CAD for VLSI and Computer Architecture.

Rooms: Flint: Ground Floor; **Quest:** 2nd Floor; **Amethyst:** Ground Floor

Final Program for July 9, 2009 (Thursday)			
08.00 AM - 09.00 AM	Registration and Breakfast		
09.00 AM - 09.30 AM	**Inauguration** **Venue:** Room - Flint		
09.30 AM - 11.00 AM	**Session 2A-1: Keynote Talk-1** **From emerging to emerged economy: Need for a Technology Infrastructure in India** **Speaker: Dr. Biswadip (Bobby) Mitra** (President and MD, Texas Instruments India) **Keynote Talk-2** **Embedded Systems: Growing complexity and augmented role of software** **Speaker: V.R.Venkatesh** (Sr. Vice President - Product Engineering Services, Wipro Technologies) **Chair: TBA** **Venue:** Room - Flint		
11.00 AM - 11.30 AM	Tea Break		
11.30 AM - 12.30 PM	**Session 2A-3** **Analog VLSI Design - 1** **Chair: K. Radhakrishna Rao** (TI India) **Venue:** Room - Flint	**Session 2B-3** **VLSI in Communication - 1** **Chair: Prasad Modali** (Intel) **Venue:** Room - Quest	**Session 2C-3** **Low Power** **Chair: Vishwani Agrawal** (Auburn University) **Venue:** Room - Amethyst
	A 1.8mW, 320MHz Sigma Delta ADC for Wireless Applications ***Harish Chandrababu**** *(IISc Bangalore), and Jamadagni H.S. (CEDT, IISc Bangalore)* 108 Regular Paper	**VLSI Implementation of Motion Vector Recovery Algorithms for H.264 based Video Codecs** ***Kavish Seth**, Muralidhar Komisetty, Vamshi Anand, Veezhinathan Kamakoti, and S Srinivasan (IIT Madras)* 19 Regular Paper	**Low-Power Adiabatic Flip-flops and Sequential Circuits using ACPL** ***Sreenu D**, Ashok Saxena, and Sudeb Dasgupta (IIT Roorkee)* 21 Regular Paper
	Clock-free Leakage-feedback Gate MTCMOS Flip-flop with a Centralized Sleep switch ***Rahul Singh**** *(IT-BHU, Varanasi)* 34 Regular Paper	**High Speed Leading One Bit Detection based New Scaling Free CORDIC Algorithm** ***Supriya Aggarwal**, Kavita Khare, and Nilay Khare (MANIT)* 8 Regular Paper	**A Novel Low Power and High Read Stability SRAM Cell** ***Sivamangai N.M** *, Saravanan P, and Gunavathi K (PSG College of Technology)* 12 Regular Paper
	CMOS Analog ASIC Design of Inverse Delayed Function Model of a Neuron for ANN *Niteen Futane, **Shubhajit Roy Chowdhury**** *(Jadavpur University), Chirasree Roychoudhuri (BESU, Shibpur), and Hiranmay Saha (Jadavpur University)* 30 Regular Paper	**Mixed-Clock Interconnect FIFO Design** ***Rakesh Yarlagadda**, Jalapally Karthik, and Hemangee Kapoor (IIT Guwahati)* 56 Regular Paper	**Peak Dynamic Power Estimation of FPGA-mapped Digital Designs** ***K Shyamala**, Shoaib Mahammad, and Veezhinathan Kamakoti (IIT Madras)* 18 Regular Paper
12.30 PM - 01.30 PM	Lunch		
01.30 PM - 03.00 PM	**Session 2A-5** **Verification** **Chair: N.S.Murty** (NXP)	**Session 2B-5** **VLSI in Communication - 2** **Chair: S.C.Bose** (CEERI Pilani)	**Session 2C-5** **VLSI in Biomedical-1** **Chair: Dinesh Sharma** (IIT B)
	Relevance of Gate Level Simulations in Today's SoC Verification ***Vishal Dalal**** *(SASKEN Communication Technologies Ltd)* 42 Short Tutorial	**Performance Evaluation of an Efficient Boolean Function Generator for Cryptographic Applications** *Debdeep Mukhopadhyay (IIT Kharagpur), and **Ankur Sharma**** *(IIT Madras)* 122 Regular Paper	**FPGA based Fuzzy Processing System for Advance Detection of Obstructive and Restrictive Pulmonary Disorders** ***Shubhajit Roy Chowdhury**, and Hiranmay Saha (Jadavpur University)* 3 Regular Paper
	Reduced Verification Effort for Low power SoC by using Right Integration, Simulation and QC Strategy *Mayank Jindal*, **Gokulakrishnan Manoharan**, Sarveswara Tammali, and Ayon Dey (Texas Instruments India)* 95 Regular Paper	**Design and Analysis of Low Power Viterbi Decoder for CDMA System** ***Ketki Joshi**, Anand Darji, and Upena Dalal (SVNIT,Surat)* Short Paper 58	**An Embedded Solution of 2-D Fast Affine Transform for Biomedical Imaging Systems** ***Pradyut Biswal**, and Swapna Banerjee (IIT Kharagpur)* 51 Regular Paper
	Addressing Via Density in UDSM Technologies using a Flexible Correct-by-Construction Approach ***Dibyendu Goswami**, Swami Gangadharan, and Albert Holguin (Intel)* 35 Regular Paper	**Design of Multiple Output, Field Programmable CMOS Voltage Reference using Floating Gate Transistors** ***Arsh Josan**, Karan Kumar, and Chota Markan (Dayalbagh Educational Institute, Agra, UP)* 118 Regular Paper	**Process, Temperature, Voltage (PTV) & Load Compensation for IOs** ***Vikas Narang**** *(Texas Instruments), Nitin Chandrachoodan (IIT Madras, Chennai), and Vinod Menezes (Texas Instruments)* 104 Regular Paper
	Virtual Platform for System Integration and Functional Test ***Praveen Kumar**** *(NXP Semiconductors India Pvt Ltd)* 6 Short Tutorial		**Ultra Low Power Digital to Analog Converter** ***Raj Dua**, Sumeet Tiwana, and Anu Gupta (BITS-Pilani)* Short Paper 65

July 9 Continued

<table>
<tr><td>03.00 PM - 03.15 PM</td><td colspan="3">Tea Break</td></tr>
<tr><td>03.15 PM - 04.30 PM</td><td colspan="3">Session 2A-6: Panel Discussion
Research and Development in VLSI/Embedded Systems
Moderator: C.P. Ravikumar, Texas Instruments India
Panelists: Ramesh N.Raghavan (GM, Wipro Technologies), M.Balakrishnan (IIT Delhi), N.S.Murthy (NXP Semiconductors)
Venue: Room - Flint</td></tr>
<tr><td>04.30 PM - 04.45 PM</td><td colspan="3">Break</td></tr>
<tr><td rowspan="4">04.45 PM - 05.45 PM</td><td>Session 2A-7
Analog VLSI Design - 2
Chair: Swapna Banerjee (IIT KGP)
Venue: Room - Flint</td><td>Session 2B-7
Digital VLSI Design
Chair: G.S.Visveswaran (IIT D)
Venue: Room - Quest</td><td>Session 2C-7
VLSI in Biomedical-2
Chair: Shyam Vasudev (Philips)
Venue: Room - Amethyst</td></tr>
<tr><td>Impact of Process Variability on 28nm Analog CMOS Performance
Ajayan K. R*, and Navakanta Bhat (IISc, Bangalore)
Short Paper 57</td><td>An Alternate Approach to Enhance Parallel Decimal Multiplier Performance
Rekha James*, K. Poulose Jacob (CUSAT, Cochi, Kerala), and Sreela Sasi (Gannon University)
4 Regular Paper</td><td>EEG-based Driving Fatigue Estimation using Discrete Wavelet Transform
Sangeeta Panigrahy* (KITS, Warangal)
Short Paper 116</td></tr>
<tr><td>A High Performance Reference Circuit using Low Input Offset Operational Amplifier
Anil Saini, and Kapil Kumar Rajput* (CEERI)
Short Paper 16</td><td>An Algorithm for High speed, Low power Implementation of Modular Multiplier
Raju Lampande*, Chandrashekhar Kukade, Raghvendra D Deshmukh, and Rajendra Patrikar (Visveswaraya National Institute Of Technology, Nagpur)
Short Paper 99</td><td>Analysis of Single Event Upset for Biomedical Applications
Surendra Rathod*, Ashok Saxena, and Sudeb Dasgupta (IIT Roorkee)
Short Paper 44</td></tr>
<tr><td>A 1.2-V 5.3–7.3GHz Wideband Quadrature LC Voltage Controlled Oscillator
Mohit Garg, M Sultan M Siddiqui, and B Bhaumik (IIT Delhi)
78 Short Paper</td><td>Hardware Implementation of Dlighting Module for using it in a Digital Camera Chip
Gaurav Agarwal*, Amit Singhal, Anu Gupta, and Prayush Kumar (BITS Pilani)
Short Paper 67</td><td>Weak Inversion based Low Power Low Noise Sixth order gm-C Filter at 1V for ECG Application with 180nm Technology
Anurag Zope*, Waman Khokle, Raghvendra D. Deshmukh, and Rajendra Patrikar (Visveswaraya National Institute Of Technology)
Short Paper 87</td></tr>
<tr><td></td><td></td><td>Switch Error and Total Harmonic Distortion Improvement Technique in SHA
Rohit Yadav* (BITS,Pilani)
Short Paper 22</td></tr>
<tr><td colspan="4">End of Day-2</td></tr>
</table>

July 10

Final Program for July 10, 2009 (Friday) - Day-3			
08.00 AM - 09.30 AM	Registration and Breakfast		
09.30 AM - 10.30 AM	**Session 3A-1: Keynote Talk-3** **Need for Energy Efficiency and Smart grids: Role of Semiconductors in future** **Speaker: Dr.Sunit Tyagi,** CEO, InSolare Energy Private Limited **Chair: TBA** **Venue:** Room - Flint		
10.30 AM - 11.00 AM	Tea Break		
11.00 AM - 12.00 PM	**Session 3A-2** **Verification** **Chair: Vineet Sahula** (MNIT Jaipur) **Venue:** Room - Flint	**Session 3B-2** **Discussion Meeting with Faculty** **Chair: C.P.Ravikumar** (TI India) **Venue:** Room - Quest	**Session 3C-2** **VLSI Test - 1** **Chair: Virendra Singh** (IISc Bangalore) **Venue:** Room - Amethyst
	VMM Methodology Template Code Generator ***Lakshman Easwaran****, Vasantha Kumar, Siva Shankar Kuppam, and Ranjith OJ (MindTree Ltd)* 11 Short Tutorial	VLSI Society of India will host a meeting of faculty and industry professionals to discuss curriculum related issues	**Bounds on Defect Level and Fault Coverage in Linear Analog Circuit Testing** ***Suraj Sindia****, Virendra Singh (IISc, Bangalore), and Vishwani Agrawal (Auburn University, Alabama, USA)* 110 Regular Paper
	A Strategy and Framework for Processor Verification ***Asheesh Shah**** *(King Saud University, Saudi Arabia), Ashwani Ramani (Devi Ahilya Vishwavidhyalaya, Indore), AbdulAziz Mazyad, and Hamid Elsemary (King Saud University, Saudi Arabia)* 112 Short Tutorial		**A Novel Test Method for Fault Detection in RF Circuits** ***Saravanan P****, Brinda Subburaj, and Kalpana Shekar (PSG College of Technology)* 9 Regular Paper
	Simulation-less Point-to-Point Connectivity Checks for SoC Environment *Venkatasreekanth Prudvi, Jayashri A B, Adwait M, Sahasrabuddhe Rajesh A Rao,* ***Sandeep Niranjan Tippannanavar*** *(IBM)* 130 Shoft Tutorial		**Prime Numbers are High Coverage Test Vectors!** ***Vasanthkumar Ramesh****, Akanksha Jain, Veezhinathan Kamakoti (IIT Madras), and Vivekananda Vedula (Intel Technology Pvt Ltd)* 74 Regular Paper
12.00 PM - 01.00 PM	Lunch		
01.00 PM - 02.00 PM	**Session 3C-4** **FPGA** **Chair: V.Kamakoti** (IIT Madras) **Venue:** Room - Flint	**Session 3A-4** **Research Scholar Forum** **Chair: C.P.Ravikumar** (TI India) **Venue:** Room - Quest	**Session 3B-4** **Low Power Design and Test** **Chair: Jais Abraham** (AMD) **Venue:** Room - Amethyst
	A High Performance Implementation of LU Decomposition on FPGA ***Manish Kumar Jaiswal****, and Nitin Chandrachoodan (IIT Madras, Chennai)* Short Paper 91	**FPGA Implementation of Visible Watermarking Processor** ***Hitendra Gupta*** *(LNMIIT), and Kamlesh Sharma (MNIT)*	**Capture Power Reduction for Modular System-on-Chip Test** ***Jaynarayan Tudu**** *(IISc, Bangalore), Erik Larsson (Linkoping University), Virendra Singh (IISc, Bangalore), and Adit Singh (Auburn University)* 120 Regular Paper
	Design of Run Time FPGA Router using JBits 3.0 *Hafizur Rahaman (Bengal Engg. & Sc. Univeristy), Nachiketa Das (Marine Engineering and Research Institute, Kolkata), and* ***Pranab Roy**** *(BESUS, Shibpur)* Short Paper 90	**TIQ Technique based Optimized Analog to digital Converter** ***Meghana Kulkarni**** *(G.I.T. Belgaum), Dr. V. Sridhar (P.E.S. College of Engineering, Mandya), and Dr. Gururaj Kulkarni (KLS Gogte Institute of Technology, Belgaum)*	**A Centralized BIST Infrastructure Design for Stuck-At Fault Detection In SoC** ***Rupsa Chakraborty****, and Dipanwita Roy Chowdhury (IIT Kharagpur)* Short Paper 69
	Constructing Synthetic Benchmark Circuits to Stress Test FPGAs ***L Srivani****, Veezhinathan Kamakoti (IIT Madras), and Ilango Sambasivam (IGCAR, Kalpakkam)* Short Paper 117	**Performance Analysis of Low power 6T SRAM Cell in 180nm and 90nm** ***Sreeramareddy G.M.*** *(S.V. College of Engg & Tech), and Ch. Chandrasekarareddy P (JNTUCE, Hyderabad)*	**Low Power Test Implementation through Temporal Spreading of Scan Shift/Capture and Q-Gating** *Pranay Kotasthane, Sireesha Arisetti, Sreeram Chandrashekar,* ***Kishore Kumar Robbi****, and Anirban Saha (Texas Instruments India)* 100 Regular Paper
02.00 PM - 02.30 PM	Break		

July 10 Continued

	Session 3C-5 **Design Automation** **Chair: C.P.Ravikumar** (TI India) **Venue:** Room - Flint	**Research Scholar Forum** **Continued**	**Session 3B-5** **VLSI Test - 2** **Chair: Adit Singh** (Auburn Univ.) **Venue:** Room - Amethyst
	How to Accommodate Design Changes using Standard Cell Library *Radhika V. Guttal, Harish Venkatesh, and **Akhtar W. Alam** (ARM Embedded Technologies)* Invited talk		**BIST / Test-Decompressor Design using Combinational Test Spectrum** *Nitin Yogi, and **Vishwani Agrawal*** *(Auburn University)* 82 Regular Paper
	Uniform Thermal Distributions in Placement of Standard Cells and Gate Arrays: Algorithms and Results ***Prasun Ghosal****, Hafizur Rahaman (Bengal Engineering & Science University), and Partha Dasgupta (IIM Calcutta)* Short Paper 72		**Synthesis of Analog Inputs for Testing of Digital Modules in Mixed Signal VLSI Circuits** ***Chiranjeevi Yarra**** *(IIT, Kharagpur), Santosh Biswas (IIT, Guwahati), and Siddarth Mukhopadhyay (IIT, Kharagpur)* 63 Short Paper
	Surface Potential Based Current Modeling of Thin Silicon Channel Double and Tri-Gate SOI FinFETs ***Robin Prakash****, Rohit Yadav (BITS, Pilani), and Subhash Bose (Central Electronics Engineering Research Institute, Pilani)* 20 Short Paper		**Performance Evaluation of Mesh-of-Tree Based Network-on-Chip Using Wormhole Router with Poisson Distributed Traffic** *Santanu Kundu (IIT Kharagpur), **Radha Purnima Dasari** * (Texas Instruments, Bangalore), Kanchan Manna, and Santanu Chattopadhyay (IIT Kharagpur)* Short Paper 61
	Simulation of Improved Dynamic Response in Active Power Factor Correction Converters ***Matada Mahesh****, and Anup Kumar Panda (NIT Rourkela)* Short Paper 77		
03.45 PM - 04.45 PM	**Session 3A-6** **Valedictory** **Chair:** **Venue:** Room - Flint		
End of Symposium			

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6th VDAT	Bangalore	August 29-31, 2002	300
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VLSI Society of India

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